https://doi.org/10.26552/com.C.2014.1.3-9

Peter Bury - Taketoshi Matsumoto - Stefan Hardon - Ivan Bellan - Marian Janek - Hikaru Kobayashi *

INVESTIGATION OF INTERFACE STATES IN Si/NAOS-SiO_2/HFO_2 STRUCTURES USING COMPLETE ACOUSTIC SPECTROSCOPY

The set of MOS structures formed on n-type Si substrate with (NAOS)-SiO_2/HfO_2 gate dielectric layers was prepared and annealed in N_2 atmosphere at various temperatures to stabilize the structure and to decrease the interface states density. Two Acoustic DLTS techniques using both surface (SAW) and longitudinal (LAW) acoustic waves including acoustoelectric response signal versus gate voltage dependence (U_{ac}-U_g characteristics) were used to characterize the interface states and the role of annealing treatment. The main interface deep centers with activation energies about 0.30 and 0.20 eV, typical for dangling bonds were observed as well as a particular influence of annealing treatment on the interface states. The obtained results are analyzed, discussed and mutually compared.

Keywords: *Acoustic DLTS, MOS structures, NAOS SiO_2/HfO_2 oxide layer, interface states.*

1. Introduction

High permittivity (high-κ) dielectrics are subject of great study in order to replace SiO_2 as gate dielectric in metal-oxide-semiconductor field-effect (MOS-FET) transistors in the future scales of integration [1]. HfO_2 is among the most promising high-κ dielectrics, but before these materials can replace SiO_2 as gate dielectric, the nature and formation of electrically active defects existing in these materials should be known because they play an important role in device operation. Moreover, HfO_2, as most of the high-k materials, when deposited in direct contact with Si an interfacial oxide layer few nanometers thick is formed [2]. One of the possible procedures to avoid reaction on Si surface is to grow a controlled free-defect SiO_2 barrier layer between substrate and high-κ dielectric. However, this barrier layer can lead to a reduction of the dielectric constant and, hence, to the effective capacitance of the gate dielectric stack, impeding to reach the necessary equivalent oxide thickness values [3 and 4].

Two basic modifications of acoustic (acoustoelectric) deep-level transient spectroscopy (A-DLTS) were introduced after the acoustoelectric effect (AE) in semiconductor structures has been shown to be one of a useful tool for the experimental study of interface states. The surface acoustic wave (SAW) technique uses a nonlinear acoustoelectric interaction between the SAW electric field and the free carriers in an interface region which generates a transverse acoustoelectric signal (TAS) across the structure [5 and 6]. The longitudinal acoustic wave (LAW) technique uses an acoustoelectric response signal (ARS) observed at the interface of the semiconductor structure when a longitudinal acoustic wave propagates through the structure [7 and 8]. Because both TAS and ARS are very sensitive to any changes in the space charge distribution in the interface region their time development after an injection pulse has been applied to the structure (A-DLTS) and their dependence on external voltage (U_{ac}-U_g curves) can be used to study the interface states properties including their activation energy, cross-section and concentration and interface states distribution [8 - 10].

In this contribution the MOS structures prepared on n-type Si substrate with SiO_2/HfO_2 gate dielectric layers formed by HfO_2 oxide deposited by atomic layer deposition on SiO_2 oxide film prepared with nitric acid oxidation of Si (NAOS) are investigated by the SAW and LAW A-DLTS techniques including the ARS – gate voltage (U_{ac}-U_g) dependences to characterize the interface states and the role of annealing treatment. The obtained results are analyzed, discussed and mutually compared.

2. Theoretical principles

The basic principle of an ARS creation can be explained using the idea of an acoustic wave passing through the MOS structure characterized by the particular space charge region at the interface. The acoustic wave, following the modulation of charge density by acoustic pressure $p = p_0 \cos(\omega t\text{-}kx)$ evokes

* [1]Peter Bury, [2]Taketoshi Matsumoto, [1]Stefan Hardon, [1]Ivan Bellan, [1]Marian Janek, [2]Hikaru Kobayashi
[1]Department of Physics, Faculty of Electrical Engineering, University of Zilina, Slovakia
E-mail: peter.bury@fel.uniza.sk
[2]Institute of Scientific and Industrial Research, Osaka University, CREST, Japan Science and Technology Organization, Osaka, Japan

the change of the potential difference that manifests as an ARS signal. The ARS produced by a MOS structure propagating by longitudinal acoustic wave can be then expressed by the relation [10 and 11]

$$U_{ac} = \varphi_s \frac{p}{K_s} - \frac{Q(\varphi_s)}{C_{ox}} \frac{p}{K_i} - \frac{Q_{it}(\varphi_s)}{C_{ox}} \frac{p}{K_i} = \\ = U_{ac}^{o} \cos(\omega t - kx) \quad , \qquad (1)$$

where φ_s is the surface potential, Q_s is the semiconductor charge, Q_{it} is the trapped charge at the interface state, C_{ox} is the oxide capacitance, K_s and K_i are the elastic moduli of the semiconductor and insulator, respectively and p_0 is the acoustic pressure amplitude.

The non-destructive SAW A-DLTS technique is based on the fact that the electric field accompanying the SAW on a piezoelectric substrate can generate the TAS that reflects any changes in the space charge distribution in the interface regions. The resulting electric field across the structure calculates dc AE effect and hf wave propagation properties and can be expressed by the relation [12]

$$E = E_0 + E_1 e^{-i(\omega t - kx)} \, , \qquad (2)$$

where E_0 is dc part and E_1 is the amplitude of hf part of TAS, respectively. The corresponding carrier density follows the relation

$$n = n^0 + n_0 + n_1 e^{j(\omega t - kx)} , \qquad (3)$$

where n^0 is the carrier concentration with no applied field and n_0, n_1 are the AE term and term proportional to the amplitude of exciting wave, respectively. The transversal hf acoustoelectric signal can be then given by the relation

$$U_{ac} = \int_0^d E_{1y} \sin(\omega t - kx) dx \, . \qquad (4)$$

Here d is the selected window width. Choosing the interaction space of the λ/2 length [or (2n+1) λ/2] in x direction, where n is the natural number, the average value is not zero any more and reaches its maximum.

The principle of A-DLTS technique [6, 8 and 10] is based on the fact that the change of the amplitude of the measured ARS, δU_{ac}^0 and/or TAS after an injection pulse has been applied is proportional to the nonequilibrium charge at the interface and the decay time constant associated with the relaxation of the ARS or TAS amplitude is then a direct measure of the time constant associated with the relaxation processes of injected carriers. Therefore, the ARS amplitude time dependence can be written as

$$U_{ac}^0(t) = U_0 + U_1 \exp(-t/\tau) \, , \qquad (5)$$

where U_0 is the original ARS (TAS) due to the acoustoelectric interaction of acoustic wave and charge at the interface of MOS structure and U_1 represents the increase of the ARS (TAS) due to the injection pulse. The time constant characterizing the relaxation processes after applied injection pulse can be expressed for electrons by the relation

$$\tau^{-1} = \gamma_n \sigma_n T^2 \exp\left[-\frac{E_a}{k_B T}\right], \qquad (6)$$

where σ_n is the capture cross section, γ_n is constant, E_a is the interface state activation energy related to the bottom of conduction band, k_B is the Boltzmann's constant and T is the thermodynamic temperature. The analysis of the time dependence of the ARS or TAS at different temperatures then allows to construct the A-DLTS spectra and following to determine the activation energy of interference states E_a and corresponding cross section σ_n [6 - 11].

If the ARS in the MOS structure without any interface states (Q_{it} = 0) is indexed as "ideal" then the ARS amplitude can be expressed [10 - 11] in the form

$$U_{ac}^0(ideal) = \left| \frac{p_0}{K_s} \right| (U_g - U_{fb}) \Big| + \frac{Q_s}{C_{ox}} \frac{K_i - K_s}{K_s K_i} p_0 \Bigg| \, , \qquad (7)$$

where U_{fb} is the flatband voltage. As it can be seen from Eq. (7) the ARS of ideal MOS structure is the superposition of linear term with zero at flatband voltage and term representing the contribution from the semiconductor charge Q_s. Comparing Eq.(1) and Eq.(7) the interface trapped charge can be expressed through the deviation of the ARS of real and ideal structures as

$$Q_{it} = S(U_{ac}^0 - U_{ac}^0(ideal)) \, , \qquad (8)$$

where $S = C_{ox} K_s / p_o$. To determine the energy distribution of interface states, it is necessary to know the dependence of the semiconductor charge on the surface potential for an ideal MOS structure. This dependence can be obtained using Terman's model [13]. The physical meaning of the absolute values is that the ARS cannot differentiate the total charge or potential polarity.

The interface state density D_{it} can be then expressed, appearing from the U_{ac}-U_g curves for ideal and real MOS structures, by the relation

$$D_{it}(E_t) = \frac{1}{q} \left| \frac{dQ_{it}}{d\varphi_s} \right| = \frac{1}{q} \left| S \frac{d(U_{ac}^0 - U_{ac}^0(ideal))}{d\varphi_s} \right| \, , \qquad (9)$$

Eq. (5) allows to determine the modeling of the distribution of interface states from the measured ARS.

However, the leakage current represented by tunneling transport in the case of very thin oxide layers (< 10 nm) becomes a significant problem. The tunneling current for very thin oxide layers influences the division of the applied voltage U_g between the semiconductor and insulator layer and for the oxide layer thickness < 2 nm the whole applied voltage practically spreads

across the semiconductor, especially in the range of inversion [14]. Concerning the tunneling process the transport of free charge curriers through the thin oxide layer caused by applied electric field has to be taken into account where the tunneling current following the Fowler-Nordheim mechanism [15] induces additional change of the ARS

$$\Delta U_{ac} = A\left(U_g^2 + B\right)e^{-\frac{C}{U_g}}, \tag{10}$$

where A, B and C are constants. The tunneling current is supposed to be dependent only on the applied voltage. The simulation of the "ideal" ARS inclusive the calculation of tunnel current contribution gives a new ideal ARS, $U_{ac}^0(tunnel)$. The interface charge can be then expressed using the new ideal and real ARS-voltage curves for MOS structure by the relation

$$Q_{it} = S\left|\left(U_{ac}^0 - U_{ac}^0\left(tunnel\right)\right)\right|. \tag{11}$$

The calculation procedure for determination of interface states density is ~~is~~ then given by Eq. (9). Except the leakage current the Schottky contact on the metal-semiconductor interface can be the reason of some deviation of the measured U_{ac}-U_g dependence, especially near the flatband. To eliminate this influence, the added capacitance of Schottky contact was included into the calculation procedure.

3. Experimental

The MOS structure prepared on n-type Si substrate wafers with NAOS-SiO_2/HfO_2 gate dielectric layer was formed by 5nm HfO_2 oxide deposited by atomic layer deposition on 0.6 nm NAOS-SiO_2 oxide film prepared in ~100% HNO_3 vapor [16]. The set of investigated MOS capacitors contained ~~such~~ original MOS structures (A1, A2) and structures ~~was~~ annealed in N_2 atmosphere at 200 (A3, A4), 300 (A5, A6) and 400 °C (A7, A8) for 10 min to stabilize the structure and decrease the leakage current density. After annealing procedure, aluminum dot electrodes were evaporated. The samples size was 2x2 cm^2 and electrodes were evaporated with diameter 2.5, 1.5 and 1.0 mm. The investigated samples list and obtained experimental results are summarized in Table 1. It should be noted that couples of samples A1-A2, A3-A4, A5-A6 and A7-A8 represent the same structures but prepared for LAW or SAW techniques, respectively.

The block diagram of the experimental setup for A-DLTS is illustrated in Fig. 1. The computer was used to trigger the apparatus, to generate excitation bias pulses as well as to record and evaluate the isothermal transients of the ARS and/or TAS. The LAW of frequency 13.2 MHz and SAW of frequency 10 MHz were generated using $LiNbO_3$ transducer and interdigital transducer evaporated on $LiNbO_3$ delay line, respectively in the arrangement illustrated in the A- and B-detail of Fig. 1. The acoustoelectric signals produced by MOS structure were after detection in the Box-car Averager recorded and stored by computer. The quiescent bias voltage pulses of 200 ms with filling traps completely were applied to the MOS structures. The ARS and TAS were monitored as a function of temperature and peaks with maxima of the temperature for which the emission rate was the same as the adjusted sample rate were observed in A-DLTS spectra [8 - 10]. The A-DLTS experimental results were at temperatures varying between 400 and 77 K, with the samples cooled in nitrogen cryostat.

To determine the interface states density the U_{ac}-U_g measurements were performed using the same acoustic equipment as for A-DLTS with the difference of bias source. Whereas for the A-DLTS the voltage source provided with bias voltage pulses, for the measurement of U_{ac}-U_g curves the voltage source provided with both the linear increase (decrease) of gate bias and the variation of increasing (decreasing) rate. Current voltage (*I-V*) and capacitance voltage (*C-V*) characteristics were observed using FLUKE PM 6306, programmable automatic RLC meter.

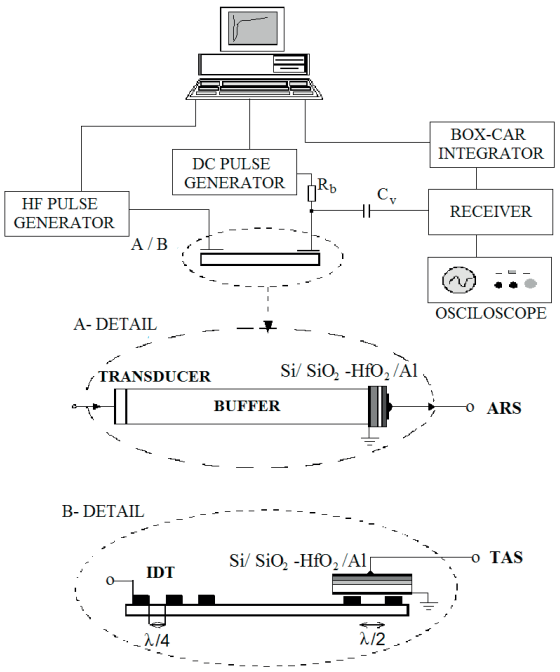

Fig. 1 Block diagram of the experimental setup for A-DLTS. The sample configuration for LAW technique is in A- detail and For SAW in B-detail

4. Results and discussion

Figure 2 shows the representative SAW A-DLTS spectrum of original Si/SiO_2/HfO_2 structure and calculated Arrhenius plot inside. The illustrated spectrum that was observed with pulse voltage ΔUg = +4.0 V (Ug = -1 V), similarly as other samples,

contains one evident peak with some lateral structure that gradually decreases from the original structure A2 to the sample A8 annealed at 400°C. Except for this "cleaning process" there was observed also some shift of the activation energy in regard to the original structure.

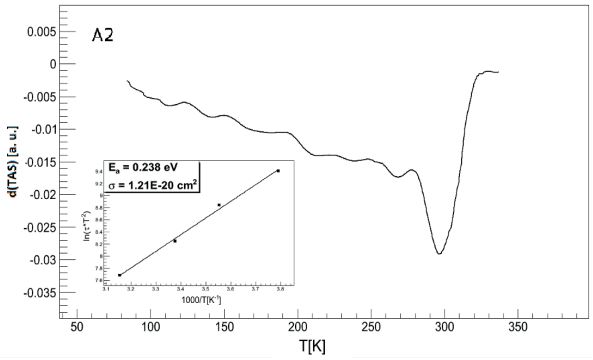

Fig. 2 SAW A-DLTS spectrum of Si/SiO$_2$/HfO$_2$ structure (A2) and calculated Arrhenius plot (inside)

Figure 3 presents a representative A-DLTS spectrum of original structure A1 obtained using LAW technique and calculated Arrhenius plot (inside). The illustrated spectrum that was observed with pulse voltage ΔU_g = +3.0 V (Ug = 0 V) contains one evident peak with some lateral structure that also gradually decreases from the original structure A1 to the sample A7 annealed at 400°C [11]. Except for this reducing process there was observed also some shift of the activation energy in regard of the original structure. Therefore, the interface quality using the interfacial SiO_2 layer seems not to be influenced by the annealing process markedly.

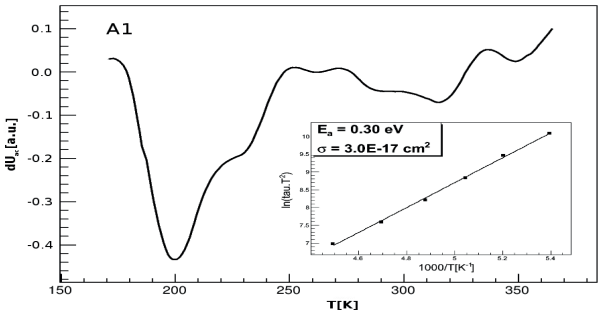

Fig. 3 LAW A-DLTS spectrum of Si/SiO$_2$/HfO$_2$ structure (A1 sample) and calculated Arrhenius plot (inside)

The results of both TAW and SAW A-DLTS are summarized in Table 1. The activation energies and corresponding cross sections of interface states were determined from the A-DLTS spectra, observed from the ARS and/or TAS amplitude transients measured at different temperatures.

The Electron Spin Resonance data [2] indicated that the basic defects observed at the Si/HfO_2 interface were identical to those found in conventional thermally oxidized silicon. However, the tunneling process from inner layer interface states is possible, too. Both kinds of interface states detected by SAW and/or LAW technique were already observed [3 and 17]. Interface states observed on Si/SiO_2/HfO_2 structures are usually attributed to isolated Si dangling bonds with which no atoms in the oxide layer interact and/or attributed to Si dangling bonds interacting weakly with an oxygen or Si atom in the oxide layer, respectively. The difference between SAW and LAW A-DLTS results can be caused by the different mechanism of SAW and LAW interaction with charge at the interface region, as well as the shift of applied voltage U_g in the case of SAW technique due to the dc transversal acoustoelectric voltage (TAV) produced by structure [5 and 12].

Summarization of the investigated Al/NAOS-SiO_2-HfO_2/Si MOS structures, activation energies and cross-sections provided by LAW and SAW A-DLTS

Table 1

	Annealing process	E_a [eV]		σ [cm^2]	
		LAW	SAW	LAW	SAW
A1	Without annealing	0.30		3.0×10^{-17}	
A2	Without annealing		0.23		1.2×10^{-20}
A3	N_2 at 200°C for 10 min	0.28		8.4×10^{-17}	
A4	N_2 at 200°C for 10 min		0.17		6.6×10^{-22}
A5	N_2 at 300°C for 10 min	0.37		4.0×10^{-16}	
A6	N_2 at 300°C for 10 min		0.20		9.8×10^{-21}
A7	N_2 at 400°C for 10 min	0.33		6.1×10^{-17}	
A8	N_2 at 400°C for 10 min		0.19		1.2×10^{-21}

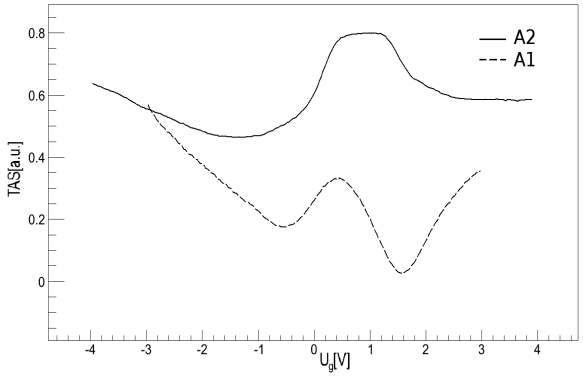

Fig. 4 Dependence of the TAS and ARS on gate voltage Ug for original structures, A1 and A2

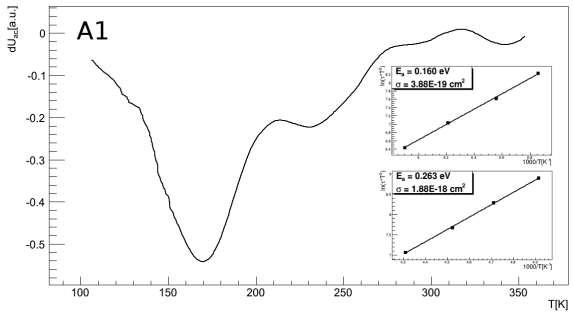

Fig. 5 LAW A-DLTS spectrum of Si/SiO_2/HfO_2 structure (A1 sample) and calculated Arrhenius plots (inside) obtained for ΔU_g = +5.0 V, U_g = -2.0 V

Figure 4 presents the dependences of the ARS as well as TAS on the gate voltage for original structures A1 and A2, respectively. Besides, the LAW technique can identify the role of interfacial SiO_2 layer (interface SiO_2/HfO_2) and corresponding tunneling, the SAW technique is not so sensitive.

However, using pulse voltage ΔU_g =+5.0 V (U_g= -2.0 V), similar as in the case of SAW spectra we found as a certain shift of A-DLTS spectra obtained for only positive voltage (ΔU_g = +3.0 V, U_g= 0 V) [11] as also some highlighting of another peak at lower temperatures (˜170 K) corresponding to the interface state with activation energy ˜0.12-0.16 eV (see Fig. 5). This fact indicates as the typical feature of interface states moreover the role of HfO_2/ SiO_2/ interlayer (IL).

The energy diagrams of the MOS structures under accumulation and inversion are illustrated in Fig. 6. We also assume that defects exist also at the HfO_2/SiO_2 IL as well as at Si/SiO_2 interface. A-DLTS measurements consist of applying accumulation pulses to fill the interface states in the upper half of the semiconductor band gap followed after reverse voltage in which the interface states emit electrons to the conduction band yielding the ARS or TAS transients that are conveniently recorded and processed to obtain the A-DLTS spectra. If the SiO_2 film is thin enough, tunneling between the semiconductor and the IL may occur. At accumulation,

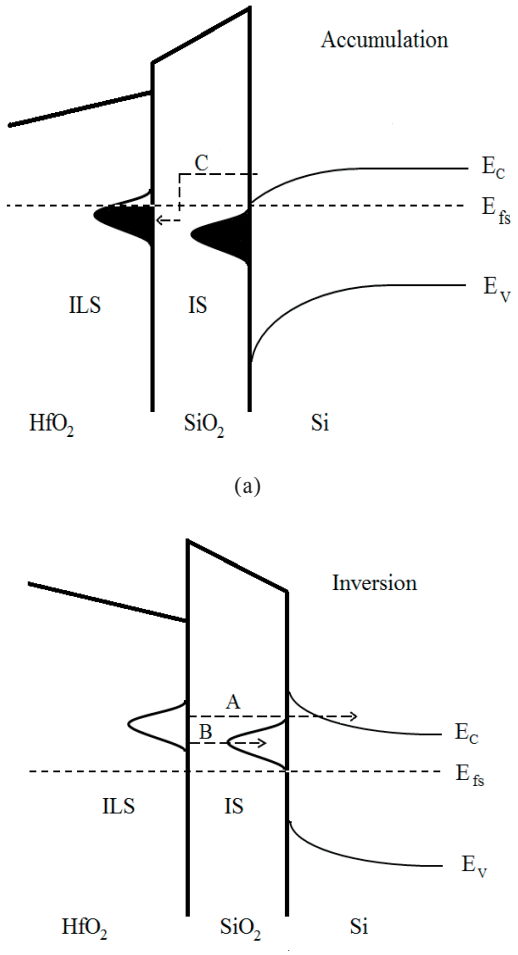

Fig. 6 Energy band diagram of Si/ SiO_2/HfO_2 structure at accumulation (a) and inversion (b)

capturing electrons coming from the semiconductor band by direct tunneling fills IL states. When the reverse pulse is applied, these defects emit the captured electrons to the semiconductor band. The emission process may occur in two different ways: IL states with energies above the silicon conduction band emit electrons by direct tunneling (A). On the other hand, for energies ranging from the Fermi level to the semiconductor conduction band tunneling between the IL states and the interface states (B) and following to the conduction band can occur. Electrons emitted according the (B) sequence increase the acoustoelectric transient, obtaining an

apparent increase in the measured interfacial state densities. Since all these mechanisms are tunneling assisted the thinner the silicon dioxide films the higher their probability. In our experiment, the SiO_2 layer thickness was 0.6 nm.

Moreover, an increase in the filling electric field in Fig. 6(a) (higher bias in the accumulation regime) causes a larger number of IL filled traps (C). Then, when biasing the sample in the inversion regime, a higher number of IL traps can contribute to the ARS or TAS transients by direct tunneling. This result agrees with results shown in [3]. On the contrary, variations in the inversion bias should not change the total filled traps, and the emitted charge from the IL traps does not change - significantly.

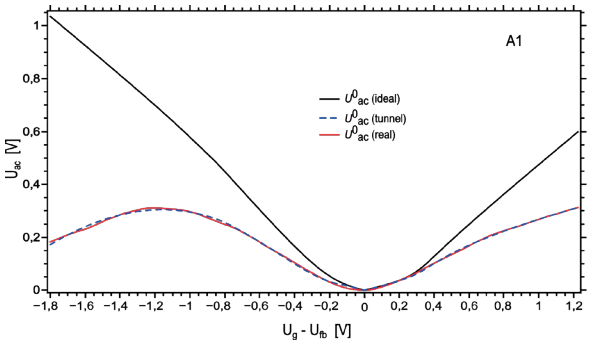

Fig. 7 Theoretical U_{ac}- U_g characteristics of "ideal" $Si/SiO_2/HfO_2$ structure without any interface states (thick line) and "ideal" structure with tunneling process (dashed line) compared with real U_{ac}-U_g curve (red line)

Figure 7 shows the measured ARS dependence on gate voltage, U_{ac}-U_g curve for sample A1 (Fig. 4) including the theoretical (ideal) U_{ac}-U_g characteristics for the $Si/SiO_2/HfO_2/Al$ MOS structure without any interface states as well as simulated characteristics for the same structure comprehensive of tunneling process. Using these real and theoretical characteristics the density of interface states could be determined (Fig. 8). We can see, in the first place, that our theoretical calculation of ideal U_{ac}-U_g curve very well coincides with real one and, secondly, that the density of interface states course corresponds to the presence of interface states with energies around ~ 0.2 – 0.3 eV detected also by A-DLTS (Table 1). The average values of density of interface states calculated using the correct value of donor concentration, N_D=4.7×10^{21} m^{-3} and considering the Schottky contact, changed from 2.64$_x$10^{12} eV^{-1}cm^{-2} (A1) up to 1.05$_x$10^{12} eV^{-1}cm^{-2} (A7).

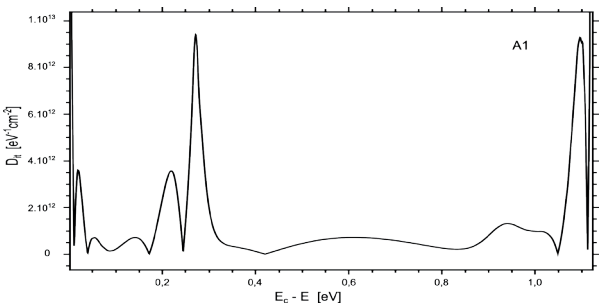

Fig. 8 Distribution of interface states calculated from U^0_{ac} - U_g characteristics for original structure (A1)

The reduction of the leakage current densities for annealed structures is evident only for the gate voltage close to zero (from –0.3 V to +0.3 V) decreasing from sample A1 gradually to sample A7 [11]. The behavior of *I-V* curves corresponds to theoretical predictions for such structures [14] but except for the mentioned interval it is almost identical for both untreated and treated structures, although there were significant differences in *C-V* characteristics. The reason of such behavior could be caused by two kinds of interface states, at both SiO_2/Si and HfO_2/SiO_2 interfaces. Then the tunneling process through the SiO_2 interfacial layer at accumulation and/or depletion can lower the influence of the annealing treatment [3 and 11]

5. Conclusion

MOS structures with HfO_2 oxide layer formed on n-type silicon with interfacial SiO_2 layer prepared by NAOS method and annealed in N_2 at various temperatures were studied by LAW and SAW acoustic spectroscopy. The main interface states with activation energy of 0.17 – 0.23 eV, observed by SAW A-DLTS are quite different from those found by LAW A-DLTS (0.27-0.37 eV) typical for dangling bonds type defects and identical to those in Si/SiO_2 interface. These differences can be caused by both the different mechanism of SAW and LAW interaction with charge at the interface region and due to the dc transversal acoustoelectric voltage produced by structure. Except for this, a post-deposition annealing at 200, 300, and mainly at 400°C leads to the reduction of interface state density, hysteresis effect as well, but only insignificantly leakage current density. The lowering influence on the characteristics of annealed MOS structures with NAOS-SiO_2/HfO_2 gate dielectric layers can indicate the stabilization role of the NAOS-SiO_2 interfacial layer. However, the next reduction should be realized by appropriate modification of structure processing steps. An observed shift of the interface state activation energies and some "cleaning" process observed in annealed structures can be explained by reduction of weak Si dangling bonds with surrounding atoms.

Acknowledgements

The authors would like to thank to Mr. F. Černobila for technical assistance and Assoc. prof. I. Jamnický for some remarks. This work was financially supported by the R&D operational program Centrum of excellence of power electronics systems and materials for their components II. No. OPVaV-2009/2.1/02-SORO, ITMS 26220120046 funded by the European Community.

References

[1] LOCQUET, J.-P., MARCHIORI, C., SOUSA, M., FOMPEYRINE, J., SEO, J. W.: *J. App. Phys.* 100, 2006, 051610
[2] STESMANS, A., AFANAS`EV, V. V.: *Appl. Phys. Lett.* 82, 2003, 4074
[3] CASTAN, H., DUENAS, S., GARCIA, H., GOMEZ, A., BAILON, L., TOLEDANO-LUQUE, M., DEL PRADO, A., MARTIL, I., GONZALEZ-DIAZ, G.: *J. Appl. Phys.* 107, 2010, 114104
[4] HEE-WOOK YOU, WON-JU CHO: *Appl. Phys. Lett.* 96, (2010) 093506
[5] ABATE, A., MAN, K. J., OSTROVSKIJ, I. V., DAS, P.: *Solid State Electronics* 36 1993, 697
[6] BURY, P., JAMNICKY, I., RAMPTON, V. W.: *Phys.* B 94, 1999, 263
[7] BURY, P., JAMNICKY, DURCEK, J.: *Phys. Stat. Sol.* A 151, 1991, 126
[8] BURY, P., JAMNICKY: *Acta Phys. Slovaca* 46, 1996, 693
[9] HOCKICKO, P., BURY, P., SIDOR, P., JURECKA, S., JAMNICKY, I.: *Communications - Scientific Letters of the University of Zilina,* 12, 2010, 44
[10] HOCKICKO , P., BURY, P., SIDOR, P., KOBAYASHI, H., TAKAHASHI, M., YANASE, T.: Cent. *Eur. J. Phys.* 9, 2011, 242
[11] BURY, P., MATSUMOTO, T., BELLAN, I., JANEŕK, M., KOBAYASHI, H.: *Applied Surface Sciences* 269, 2013, 50
[12] FRITZ, I. J.: *J. Appl. Phys.* 52, 1981, 6749
[13] NICOLLIAN, E. M., BREWS, J. R.: MOS (Metal Oxide Semiconductor), Physics and Technology, New York : Wiley, 1982.
[14] RACKO, J., VALENT, P., BENKO, P., DONOVAL, D., HARMATHA, L., PINTES, P., BREZA, J.: *Solid State Electronics* 52, 2008, 1755.
[15] WEINBERG, Z. A.: *Solid State Electronics* 20, 1977, 11.
[16] ASUHA, A., YUSA. T., MAIDA, O ., KOBAYASHI, H.: *Appl. Phys. Lett.* 80, 2002, 4175.
[17] MASSON, P., AUTRAN, J.-L., HOUSSA, M.: *App. Phys. Lett.* 81, 2002, 3392.