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DIELECTRIC PROPERTIES AND BREAKDOWN OF THE GATE OXIDE IN THE MOS STRUCTURE

The article treats the methodology of measuring the breakdown voltage on Si-based MOS structures. Identification of defects in the thin gate oxide is performed using the Weibull statistical analysis. By comparing the current and capacitance measurements on MOS structures we determined the influence of the defect charge in the oxide upon the parameters characterizing the breakdown. A higher occurrence of defects was correlated with elevated values of the flat band voltages. This verifies the hypothesis of an increased destruction of MOS structures caused by electrically active defects arising in the course of thermic oxidation and pre-oxidation treatment of the surface of silicon.

1. Introduction

In unipolar semiconductor technology, the preparation of a high quality gate insulating layer plays an important role. In silicon technology the thin SiO_2 layer is prepared by thermic oxidation. The properties of this insulating layer and of its interfaces with silicon affect the performance of unipolar devices and integrated circuits markedly [1].

The fundament of unipolar circuits is the MOS (Metal Oxide Semiconductor) structure. Its diagnostics is performed by current and capacitance methods [2]. The progress and utilization of theses methods determine the new trends in technology. The steep growth in the density of integration while keeping the performance parameters requires ever thinner SiO_2 layers. The properties of such thin layers strongly depend on the type and distribution of defects in the oxide. The defect charge in the oxide deteriorates the overall stability of MOS structures and increases the threshold and leakage currents. For eliminating these undesirable phenomena it is inevitable to know the type of defects and their electric activity.

The measurement of the breakdown voltage properly completes the analysis of defects in the oxide, and under certain measuring conditions and statistical evaluation of the measured data allows their identification.

We discuss the methodology of time independent measurement of the breakdown voltage (TZDB, Time Zero Dielectric Breakdown) employing the Weibull statistics for data evaluation. In accordance with the JEDEC Standard JESD35-A (Procedure for the Wafer-Level Testing of Thin Dielectrics) [3] the method is divided into the V-RAMP test (linear growth of the voltage and measurement of the current) and the J-RAMP test (exponential growth of the current and measurement of the voltage). The V-RAMP test is used to characterize defects in weak electric fields. On the other hand, the J-RAMP test is suitable for analysis of defects that manifest themselves in strong electric fields and for MOS structures with small areas of the gates.

The model of the electric breakdown of thin insulating layers becomes gradually more sophisticated. The first model believed that the cause of breakdown was impact ionization due to charge carriers injected from the gate electrode through the insulator into the substrate. A model followed of electron-hole generation in which the breakdown was assumed to be caused by a conductive channel consisting of high-density defects generated by the increased current of injected charge carriers. In this case one can also assume an effect of predominantly positive induced mobile ions in the insulating layer. The advanced model considers a simultaneous existence of several processes. The methodology of measuring the time dependent breakdown is suitable for their separation.

The latest knowledge on the breakdown mechanism of the insulating layer in the MOS structure are utilized in two models: thermo-chemical, the so-called linear *E*-model of the electric field [4], and the model of hole generation, the so-called reciprocal $1/E$ model of the electric field [5]. They assume that the electrons that can tunnel through the potential barrier of the insulating layer may induce a local increase of the electric field *E* in the layer. The places with a critical value of the electric field E_{cri} trigger the breakdown.

2. Measurement and Evaluation Methodology

For optimizing the methodology of measuring the breakdown voltage V_{BD} we used sample G00T with MOS structures containing a thin gate oxide layer. The N-type (100)-oriented silicon substrate had a resistivity of 2–5 Ωcm. The SiO_2 layer grown at a temper-

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ature of 1050 °C in dry O_2 had a thickness of $t_{OX} = 28$ nm. Aluminium gates were sputter deposited and patterned photolithographically using a CV mask with various areas of the gates, A_G. The oxide was removed from the back side of the Si wafer and a good Al ohmic contact was sputter deposited. Finally, stabilizing annealing was performed in $N_2 + H_2$ at 450 °C for 30 minutes. Figures 1a, b compare the two methods of breakdown measurement on the same wafer with MOS structures using the Keithley 237 instrument.
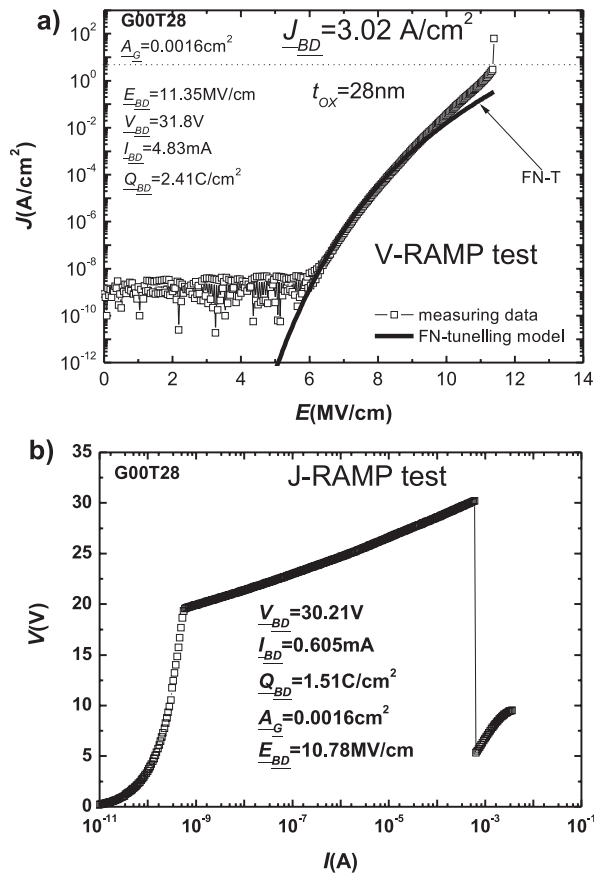

Fig. 1 Breakdown measurement:
a) V-RAMP test, b) J-RAMP test

In the V-RAMP test, the measured values are given directly by a purpose written code. A voltage of such polarity is applied to the structure that brings it into accumulation and the current is measured that flows through the gate oxide. As long as breakdown does not occur, the charge accumulated in the oxide can be expressed as

$$Q_{BD} = \sum_{i=1}^{i=N} I_{meas}(i) t_{step},$$ (1)

where I_{meas} is the current measured at the time step t_{step}, and N is the number of time steps prior to the breakdown. As a criterion of breakdown, such a current was used exceeds the value of

$$I_{BD} = 10 I_{exp}.$$ (2)

A typical value of I_{exp} is between 20 and 30 A/cm². If this current is too small, a breakdown need not occur at all. On the contrary, if I_{exp} is too large, the breakdown will not be detected because the series resistance of the structure begins to play a significant role that decreases the value of I_{BD}. The second criterion of breakdown is based on the change of the slope of the I-V curve. If the slope exceeds a certain (2 to 5-fold) value of the initial slope, one detects the breakdown.

In MOS structures with thermic SiO_2 one can assume the Fowler-Nordheim charge transport through the oxide. This model is applicable if the field intensity ranges from 6 to 10 MV/cm. The current density can be written as

$$J_{FN} = A E_{ox}^2 \exp\left(\frac{-B}{E_{Ox}}\right)$$ (3)

where

$$A = \frac{q^3 (m/m_{ox})}{8\pi h} \frac{1}{\Phi_B} = 1.54 \times 10^{-6} \frac{m}{m_{ox}} \frac{1}{\Phi_B},$$ (4)

$$B = \frac{8\pi \sqrt{2 m_{ox} \Phi_B^3}}{3qh} = 6.83 \times 10^7 \sqrt{\frac{m_{ox} \Phi_B^3}{m}}.$$ (5)

Here, m_{OX} is the effective mass of electrons in the oxide, m is the free electron mass and Φ_B is the barrier height at the Si/SiO_2 interface. Equation (3) can be written as

$$\ln\left(\frac{J_{FN}}{E_{ox}^2}\right) = \ln(A) - \frac{B}{E_{ox}}$$ (6)

whereby we get the Fowler-Nordheim formula $\ln(J_{FN}/E_{OX}^2) = = f(1/E_{OX})$. The barrier height Φ_B is obtained from the slope of the line fitted through the measured dependence.

For getting the characteristic breakdown parameters, statistical evaluation methods are used. This assumes a large set of measurements with acceptable uniformity of the parameters across the wafer. Problems may occur in the case of a small amount of measured structures on the wafer. The minimum number of measurements is 30.

The most often exploited method of statistical evaluation is the Weibull distribution. This is characterized by two functions, probability density function (PDF) and cumulative density function (CDS). We used the CDF that has the form

$$F(x) = 1 - \exp\left[-\left(\frac{x}{\theta}\right)^b\right],$$ (7)

where θ is the characteristic time (scale parameter) and b is the Weibull slope (shape parameter). Formula (7) can be written as

$$\ln(-\ln(1 - F(x))) = b(\ln(x)) - b(\ln(\theta)),$$ (8)

which is the so-called Weibull graph, see Fig. 2. The change in the slope (b) of the curve allows to determine the nature of the break-

down. The extrinsic breakdown is caused by defects created during the technology (metallic impurities, vacancies, clusters),
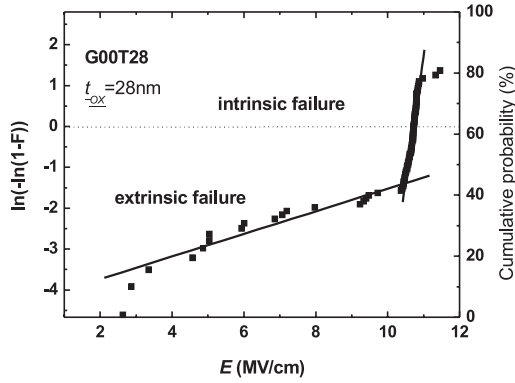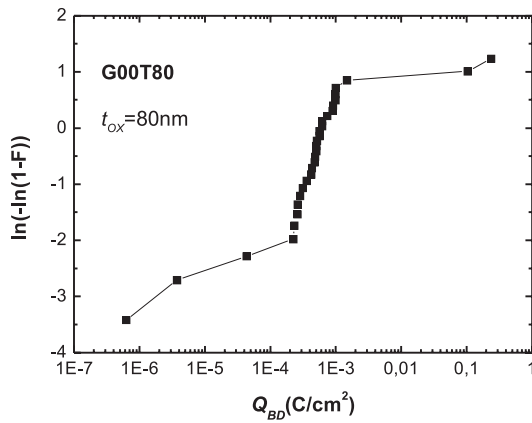

Fig. 2 The Weibull graph for sample G00T28

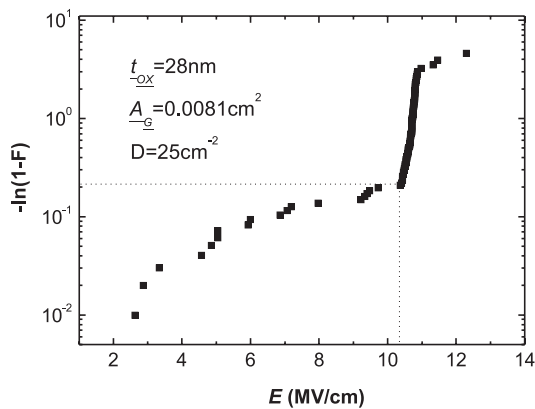*Fig. 3 Distribution of the accumulated charge displayed as a Weibull graph*

Fig. 4 Defectiveness in dependence on the field strength

intrinsic breakdown is due to primary defects inevitably created during thermic oxidation.

A useful parameter characterizing the breakdown is the accumulated charge Q_{BD} that can be shown graphically as in Fig. 3.

The distribution of the accumulated charge allows to detect those defects that are not seen in the graph showing the distribution of the electric field E_{BD}.

In unipolar technology the defectiveness in the wafer is regularly checked by measuring the breakdown voltage and statistical evaluation. For calculating the defectiveness the following formula is used:

$$F = 1 - \exp(-A_G D), \tag{8}$$

where A_G is the area of the MOS structure and D is the defectiveness. If we again rewrite function F into the form

$$-\ln(1 - F) = A_G D, \tag{9}$$

it is possible to construct the graph shown in Fig. 4. It allows to find the defectiveness at various field intensities. The defectiveness is often read at the kink of the curve between the intrinsic and extrinsic parts of defects.

3. Breakdown of MOS Structures with Various Flat Band Voltages

The effect of the defect charge of mobile ions and traps in the SiO_2 insulating layer and at the interfaces with the silicon substrate and the metallic gate of the MOS structure upon the breakdown voltage was observed on two series of samples. The first series (G00P) are MOS structures with a small value of the flat band voltage V_{FB}. In this case the density of defects in the oxide is low. The other series (G00R) are MOS structures with a large-scale value of V_{FB}, thus with a high density of defects in the oxide.

The MOS structures were prepared in the production as test samples, thus they might be contaminated in the course of Al gate sputtering. The SiO_2 gate oxide was created by thermic oxidation in $O_2 + HCl$ at a temperature of 1060 °C for 30 minutes. The substrate was N-type (100)-oriented silicon with resistivity from 2 to 5 Ωcm. After sputter depositing the back Al ohmic contact the structures were annealed in $N_2 + H_2$ at 450 °C for 30 minutes.

The quality of MOS structures was checked by *C-V* measurements. The concentration of impurities N_{sub} and the total density of defect charge N_{eff} were determined from the flat band voltage V_{FB}. Figure 5 shows the high-frequency *C-V* curves of G00P and G00R samples.

The MOS structures of G00R sample have a high negative value of the flat band voltage ($V_{FB} = -2$ V). The total defect charge was positive with a high density, $N_{eff} = 5.3 \times 10^{11}$ cm^{-2}. High quality MOS structures of G00P sample have a flat band voltage $V_{FB} = -0.1$ V, which is related to the low total positive defect density, $N_{eff} = 2.4 \times 1010$ cm^{-2}.
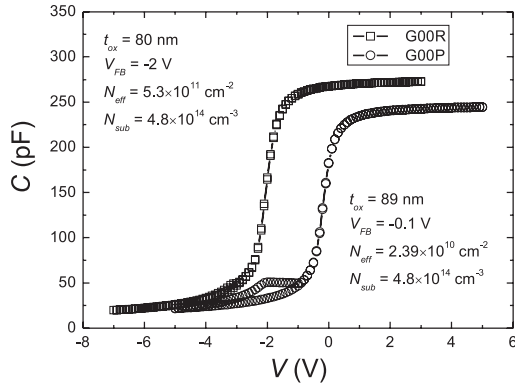
Fig. 5 Voltage dependence of the capacitance of MOS structures with various values of the flat band voltage.

Fig. 7 Weibull distribution of the measured breakdowns allowing to identify the type of defects from the shape and value of the cumulative charge

The influence of the defect charge in the oxide was assessed by measuring the breakdown voltage and evaluating the data by the Weibull statistics. In Fig. 6 one can distinguish the extrinsic region characterized by defect that had been created in the process of Si surface treatment and during thermic oxidation. These include mainly metallic impurities, traps in the bulk and mobile ions that accelerate creation of a conductive path through the oxide. In this case we observed breakdowns at field intensities up to 9 MV/cm for sample G00P and 9.3 MV/cm for sample G00R.
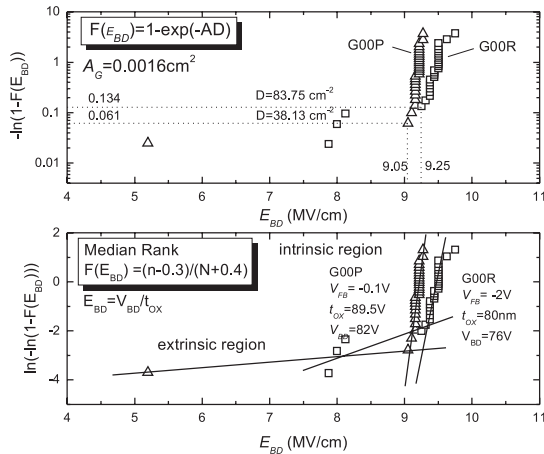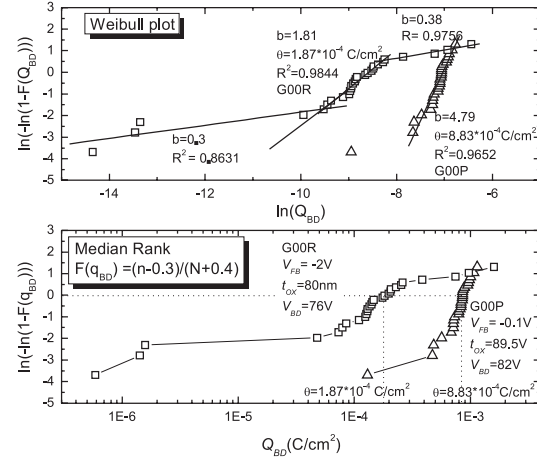

Fig. 6 Weibull distribution of the measured breakdowns expressing the defectiveness D, and classifying the defects into intrinsic and extrinsic

For the intrinsic region, breakdowns are typical due to breaking the oxygen-silicon bonds. Such traps contained in the bulk of SiO_2 and at the SiO_2/Si interface are electrically active generation-recombination centres. By means of these traps a sharp increase in the magnitude of current occurs, up to a breakdown [6].

From the Weibull analysis (Fig. 6) we deter-mined the defectiveness 33 cm^{-2} for sample G00P and 89 cm^{-2} for sample G00R.

The values were evaluated for the kink on the curve, where the extrinsic region changes into the intrinsic region.

Applying the Weibull analysis, the slope of the curve was found to be $b = 1.81$ for sample G00R and $b = 4.79$ for sample G00P with characteristic charge values $\theta = 1.87 \times 10^{-4}$ C/cm^2 (G00R) and $\theta = 8.83 \times 10^{-4}$ C/cm^2 (G00P). The slope expresses the type of defects taking part in the breakdown. The slope below 2 is typical for a breakdown caused by defects having their origin in the production (traps in the bulk of SiO_2, metallic impurities). This type of defects was detected in sample G00R. If the slope is larger than 2, it suggests defects caused by rapid wear out or fatigue of the material. In the case of breakdowns of the insulating layer, such defects can be classified in the intrinsic region. A steeper curve (smaller dispersion of the measured parameters) means a higher quality of the oxide. The Weibull analysis of the insulating layer allows to conclude that SiO_2 in sample G00P is of higher quality in comparison with that in sample G00R, as confirmed also by capacitance measurements. The MOS structures with a large defect charge (G00R) exhibited a lower quality also from the point of view of the breakdown voltage.

3. Conclusion

In semiconductor industry, the quality of the gate SiO_2 oxide in the MOS structure is checked by measuring the breakdown voltage and by capacitance methods. It has been proved that a large change of the defect charge measured by capacitance techniques does not mean a marked variation in the breakdown voltage. The Weibull analysis, however, allows to identify the type of defects and their non-uniform distribution on the wafer. Good correlation between capacitance and current measurement was not achieved before the type of defects had been determined. The samples with high values of the flat band voltage, thus with a large defect charge in the oxide exhibited also a high defectiveness. Such wafers do

not reach a satisfactory quality required for the unipolar CMOS technology.

Acknowledgement

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