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A HIGH EFFICIENCY INTERLEAVED PFC FRONT – END CONVERTER FOR EV BATTERY CHARGER

Nowadays, an increasingly present application in the automotive field is the battery charger that usually consists of two high efficiency parts: an AC/DC converter with power factor correction (PFC) capability and a DC/DC converter. In this paper, a three-channel interleaved Power Factor Correction (PFC) based on a new digital controller STNRGPF01 operating in Continuous Conduction Mode (CCM) is presented addressing high efficiency. In the considered applications, the most challenging control issues are the input current control and the fast overcurrent protections. Exploiting mixed signal control approach some benefits have been obtained and confirmed by experimental results on a 3 kW prototype.

Keywords: *active front-end, interleaved converters, battery charger, power factor correction, digital control*

1. Introduction

For electric vehicle manufacturers (EVs) and for the consumer market it is important to have high efficiency and high power chargers to optimize charging times. The charger consists of an AC/DC used as power factor correction (PFC), and a DC/DC to adapt the voltage levels to the battery type. If the efficiency of each part is greater than 97%, the overall efficiency of the battery charger will be 94% higher, unlike most of the chargers on the market [1].

In many high power applications active Power Factor Corrector (PFC) converters are widely used as the first stage in AC/DC conversion in order to meet the IEC 61000-3-2 standard for electrical equipment [2].

In order to charge the battery pack of Electrical Vehicles (EVs) from the grid, a battery charger with unity power factor correction (PFC) capacity is required. For the on-board charger (OBC) with two-stage structure [3], the front-end PFC AC/DC converter is used to rectify the input supply from AC form to DC form while controlling the input current of converter to be in phase with the input voltage, therefore, high power factor control is achieved to minimize the negative effect of OBC on the power quality of the grid. The result consists in an electrical appliance that work virtually as a pure resistive load thus the overall grid efficiency can be improved.

The conventional boost topology is the most popular topology used to realize PFC and ac/dc conversion in the power range of a few kilowatts. Generally, the converter is controlled based on the conventional dual closed-loop PI control, among which an external voltage loop regulates the output voltage and generates the reference current and an internal current loop shapes the input current to achieve the unity power factor correction [4].

In applications of power greater than 1 kW, interleaved converters are often used. Interleaving of PFCs consists of paralleling two or more active stages (Figure 1), each rated for a fractional power, instead of a bigger one rated for the full power. During normal operation the PWM driving signals are out of phase of a proper value according to sequent equation:

$$phase\ shift = \frac{360^{\circ}}{number\ of\ channels} \tag{1}$$

The benefits of the interleaved topology [5], compared to traditional single-stage PFC, are measured in terms of:

- Input current ripple reduction
- EMI filter volume reduction
- Inductor volume reduction
- Output capacitor RMS current value reduction
- Better power management for the switches
- higher efficiency thanks to channels power management

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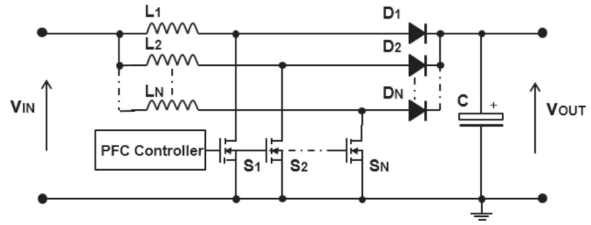

Figure 1 *Interleaved boost PFC with N active channels*

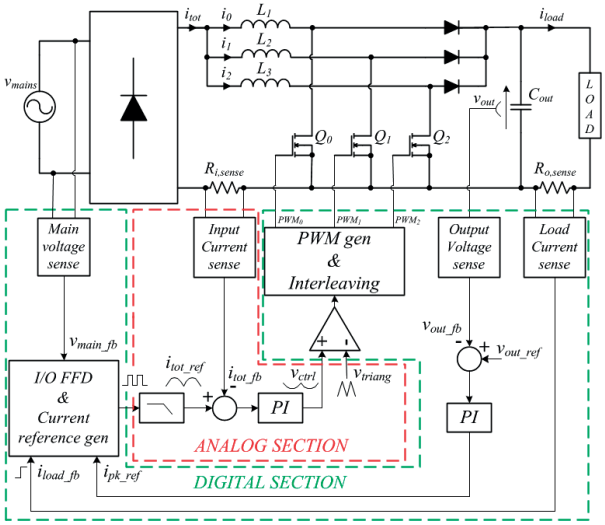

Figure 2 *IPFC mixed signal control scheme*

2. Mixed signal concept

If only Analog ICs are used, generally it not allows to totally fulfill the multi specification of power converter. For such a reason, full digital solutions are often preferred to analog ones for their flexibility and programmability. Consequently, costly microcontrollers with high computational power are needed to meet the high bandwidth requested by the current control loops. Moreover, full digital control has bandwidth limitations compared to analog implementation [6 - 8].

As a consequence, the mixed-signal control represents a good compromise because it provides at the same time the flexibility of digital solution and the dynamics of analog controllers. For the addressed application, the proposed control scheme is shown in Figure 2 [9].

An outer voltage control loop is used to set the PFC bus voltage to a reference value while an inner current loop regulates the value of the total average inductor current. A digital PI regulator calculates the peak of total input average current ipk_ref by considering the difference between the output voltage feedback Vout_fb and the reference Vout_ref. In this scheme, the PFC current reference is obtained from the I/O Feed Forward (I/O FFD) block exploiting a PWM waveform filtered using a low pass analog filter to achieve the pre-modulation reference waveform. Then, the difference between the current reference itot_ref and

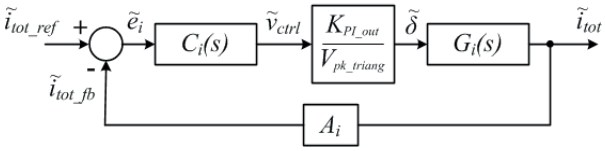

Figure 3 *PFC current control loop block diagram*

the input current feedback itot_fb is processed by an analog PI controller whose output vctrl is compared with a triangular wave Vtriang at the switching frequency to generate the master signal PWM0. In Figure 2, the digital and analog sections are highlighted by the green and red dashed line respectively. Input and load feed-forward control are used to ensure fast dynamic response when main voltage changes suddenly or a load current step occurs. Moreover, in order to obtain an almost flat figure of merit a phase shedding function is implemented in order to enable/disable the slave channels according to the load.

3. Theoretical analysis of control loops

3.1 Current control loop design

The small-signal transfer functions of the interleaved boost converter are obtained using the State-Space Averaging (SSA) method and a linearization operation (Taylor's series around an operating point) [10, 11]. In order to simplify the problem, the following assumption has been considered:

- Converter CCM operation
- Ideal active and passive components
- The three boost inductors show identical parameters and the total power is equally split among the channels
- The grid voltage is assumed to be stable during several switching cycles.

In the following equations the notation '~' specifies small-signal variables while the uppercase letter indicates quantities operating in steady-state. The control-to-input current transfer function is shown in Equation 2.

$$G_i(s) = \frac{\tilde{i}_{tot}}{\tilde{\delta}} = \frac{C_{OUT}V_{OUT}^3 s + P_{OUT}\left(1+\frac{1}{\eta}\right)V_{OUT}}{C_{OUT}L_{PFC}V_{OUT}^2 + L_{PFC}P_{OUT}s + N_{ch}V_{IN}^2} \quad (2)$$

The current control loop block diagram is shown in Figure 3.

Where Vpk_triang is the peak to peak voltage of the triangular carrier and KPI_out is a scaling factor that allow to match the PI regulator maximum output voltage value with that of the triangular carrier peak.

Ai is the input current sensing gain and Ci(s) is the compensator transfer function. The open loop compensated transfer function is then given by:

$$T_i(s) = C_i(s)\frac{K_{PI\_out}}{V_{pk\_tirang}}A_i G_i(s) \quad (3)$$

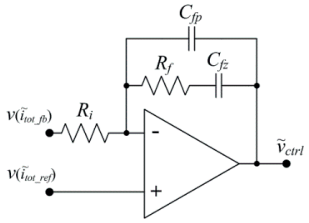

Figure 4 *Type II compensation amplifier*

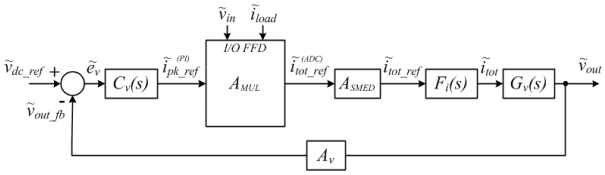

Figure 5 *Complete cascaded control loop block diagram*

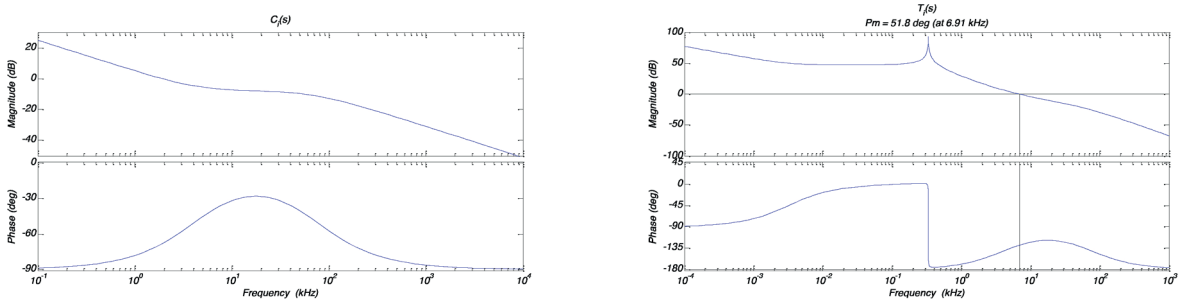

Figure 6 *Bode diagrams of current compensator $C_i(s)$ and current open loop $T_i(s)$ transfer functions*

where the typical PI controller transfer function is $C_i(s) = (K_{P\_Itot}s + K_{I\_Itot})/s$. Based on general Bode criteria equation - Equation (4) ensure system stability for a desired bandwidth ω_{Ti_des} (crossover pulsation) and phase margin PM_{i_des} and the PI controller parameters can be calculated from Equation (5)

$$\begin{cases} |T_i(j\omega_{Ti\_des})| = 1 \\ \angle T_i(j\omega_{Ti\_des}) = -180° + PM_{i\_des} \end{cases} \tag{4}$$

$$\begin{cases} K_{I\_Itot} = \dfrac{\omega_{Ti\_des}}{|L_i(j\omega_{Ti\_des})|\sqrt{1+\tan^2(PM_{i\_des} - 90° - \angle L_i(j\omega_{Ti\_des}))}} \\ K_{P\_Itot} = \dfrac{K_{I\_Itot}\tan(PM_{i\_des} - 90° - \angle L_i(j\omega_{Ti\_des}))}{\omega_{Ti\_des}} \end{cases} \tag{5}$$

Typically, the crossover frequency is selected within the range 2 - 10 kHz [12], while phase margin 45 - 60 degrees.

Since the current controller is implemented with analog type - II compensation amplifier (Figure 4) the transfer function of this compensator is given by Equation (5).

$$C_i(s) = \frac{1}{(C_{fz}+C_{fp})R_i}\frac{C_{fz}R_f s + 1}{s\left(\dfrac{C_{fz}C_{fp}R_f}{C_{fz}+C_{fp}}s + 1\right)} \tag{6}$$

3.2 Voltage loop design

The input current-to-output voltage transfer function is specified in Equation (7):

$$G_v(s) = \frac{\tilde{v}_{out}}{\tilde{i}_{tot}} = \frac{2\left(N_{ch}V_{IN} - \dfrac{P_{OUT}}{\eta V_{IN}}L_{PFC}s\right)V_{OUT}^2}{C_{OUT}V_{OUT}^3 s + P_{OUT}\left(1+\dfrac{1}{\eta}\right)V_{OUT}} \tag{7}$$

voltage loop crossover frequency is generally selected in the range 5 - 15 Hz [12], thus the right half plane zero (higher frequency) can be neglected. The cascaded control block diagram is shown in Figure 5.

where:

F_i(s) = Input current closed-loop transfer function

C_v(s) = Output voltage compensator transfer function

A_{MUL} = Digital multiplier gain for digital current reference generation

A_{SMED} = Digital to analog gain for analog current reference generation

A_v = Output voltage sensing gain

The I/O FFD block can be simply considered as a constant gain block A_{MUL}. The output voltage loop regulation is done with a digital PI controller:

$$C_v(s) = \frac{K_{P\_Vdc}s + K_{I\_Vdc}}{s} \tag{8}$$

Considering the open loop compensated transfer function shown in Equation (9):

$$T_v(s) = C_v(s)A_{MUL}A_{SMED}F_iG_v(s)A_v \tag{9}$$

and that stable system is obtained if the two following conditions are verified:

$$\begin{cases} |T_v(j\omega_{Tv\_des})| = 1 \\ \angle T_v(j\omega_{Tv\_des}) = -180° + PM_{v\_des} \end{cases} \tag{10}$$

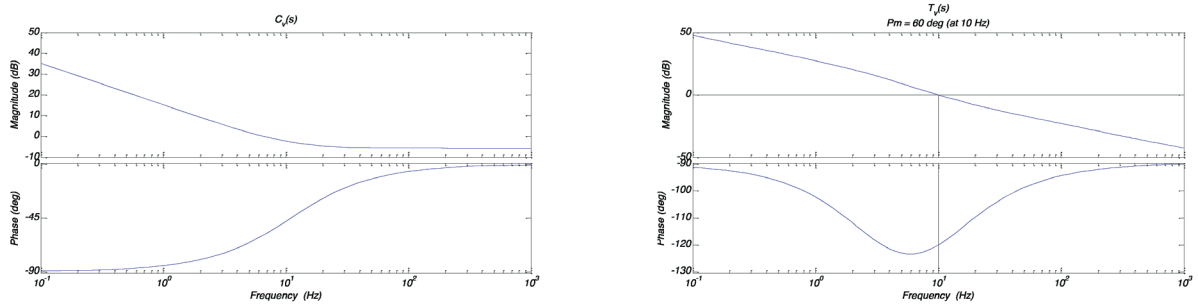

Figure 7 *Bode diagrams of voltage compensator $C_v(s)$ and voltage open loop $T_v(s)$ transfer functions*

Table 1 3 kW three-channel IPFC prototype specifications

Design parameter	Description	Value
P_{OUT}	output power	3 kW@230 Vac
N_{ch}	Number of channels	3
V_{IN}	rms nominal input voltage	230 V
V_{OUT}	rms nominal output voltage	400 V
f	line frequency	50 - 60 Hz
η	estimated efficiency	98 %
L_{PFC}	single channel boost inductor	120 µH
C_{OUT}	output capacitor	4x470 µF
V_{pk_triang}	peak-to-peak voltage of triangular wave	2 V
K_{PI_out}	PI out scale factor	0.5909
A_i	Input current sensing gain	0.0927
A_v	Output voltage sensing gain	1.9128
A_{MUL}	Digital multiplier gain	3.3086
A_{SMED}	Digital to analog gain	0.00068
f_{sw}	Switching frequency	111 kHz
f_{Ti_des}	Current loop crossover frequency	7.5 kHz
f_{Tv_des}	Voltage loop crossover frequency	10 Hz
PM_{i_des}	Current loop phase margin	60°
PM_{v_des}	Voltage loop phase margin	60°

The compensator parameters can be obtained by solving the following system:

$$\begin{cases} K_{I\_Vdc} = \dfrac{\omega_{Tv\_des}}{|L_i(j\omega_{Tv\_des})|\sqrt{1+\tan^2(PM_{v\_des}-90°-\angle L_v(j\omega_{Tv\_des}))}} \\ K_{P\_Vtot} = \dfrac{K_{I\_Vdc}\tan(PM_{v\_des}-90°-\angle L_v(j\omega_{Tv\_des}))}{\omega_{Tv\_des}} \end{cases} \quad (11)$$

Finally, according to Table 1 specifications, Figure 6 and Figure 7 show respectively the Bode diagrams for current and voltage loops. Because of the high-frequency pole and standard passive components values the actual phase margin and crossover frequency of Ci(s) are lower than the target values (60°, 7.5 kHz), therefore it has to be compensated by imposing a slightly larger value as specific.

4. Experimental results

A 3 kW three-channel IPFC prototype, showed in Figure 8, has been designed and realized in order to test the proposed control scheme, according to the following specifications - see Table 1.

The power density of 52 W/inch^3 is achieved exploiting a compact layout and the small size of magnetic components related with the benefits of interleaving and high switching frequency.

Figure 9 shows the inductor currents waveforms in small time scale. The interleaving operation is properly set with 120 degrees of phase shift.

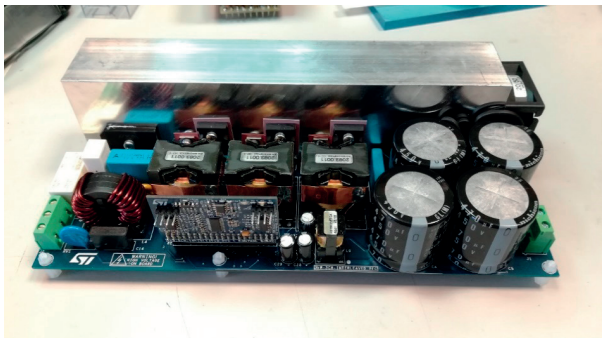

Figure 8 *3 kW 3-channel interleaved PFC prototype*

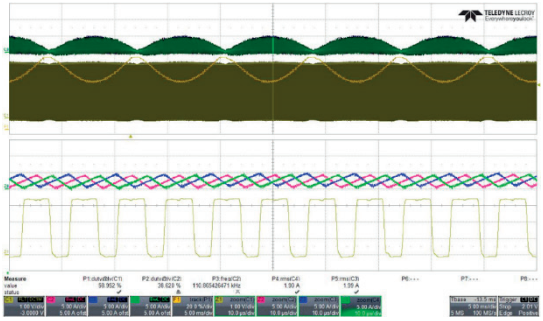

Figure 9 *Inductor current waveforms at switching frequency*

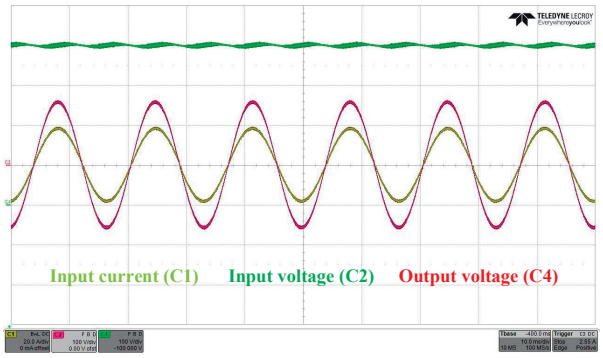

Figure 10 *IPFC at 1.5 kW (115 Vac, 60 Hz)*

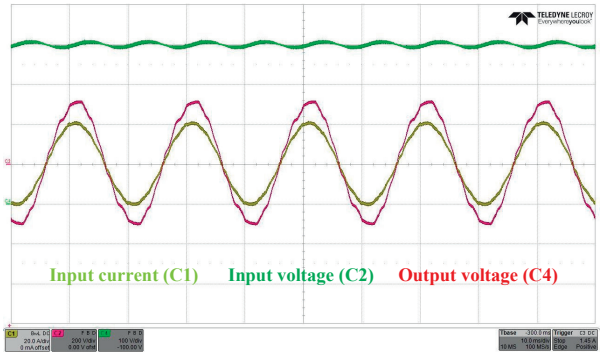

Figure 11 *IPFC at 3 kW (230 Vac, 50 Hz)*

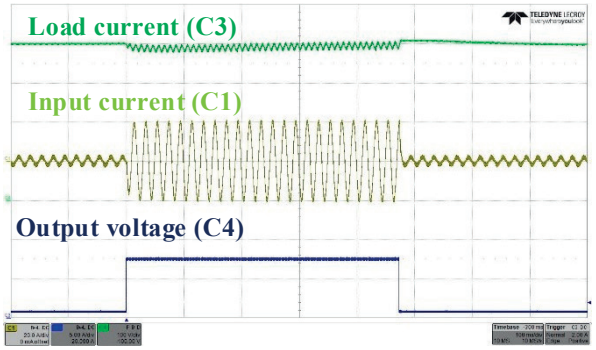

Figure 12 *10 % - 100 % - 10 % load transition*

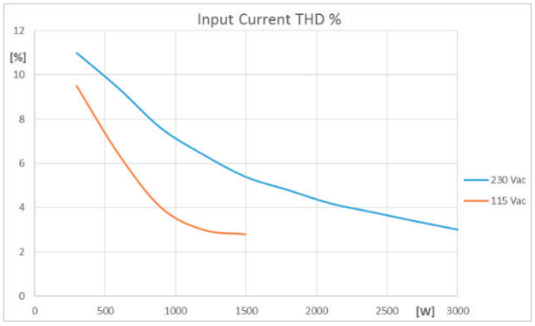

Figure 13 *Input Current THD %*

The waveform in steady state at line frequency are shown in Figure 10 and Figure 11. The board is supplied by a power AC source at 115 Vac and the power is de-rated for thermal reasons down to 1.5 kW while it is 3 kW when connected to the 230 Vac grid. The input current faithfully follows the reference thus an almost sinusoidal shaped waveform with near unity power factor is obtained even in case of line voltage distortion.

The control fast dynamic response is clearly stated in Figure 12 where a load step from 10 % to 100 % and again to 10 % is considered. Thanks to the load feed-forward the output voltage fluctuations during load transitions have been reduced.

In steady state condition THD, PF and efficiency performance are evaluated. Figure 13 shows a THD lower than 10 % at loads higher than 20 %. It decreases down to 3 % at full load for 230 Vac and below 3 % for 115 Vac. High power factor (> 0.99) is achieved from 20 % load.

Finally, a high and nearly flat efficiency has been obtained and showed in Figure 14 thanks to the phase shedding operation. Its value is about 97.6 % from 50 % to 100 % load.

5. Conclusion

For automotive application of PFC AC/DC converter to be used as front-end stage in battery charger, a new approach is presented combining mixed signal control and phases interleaving that allows to match at the same time the advantages of analog

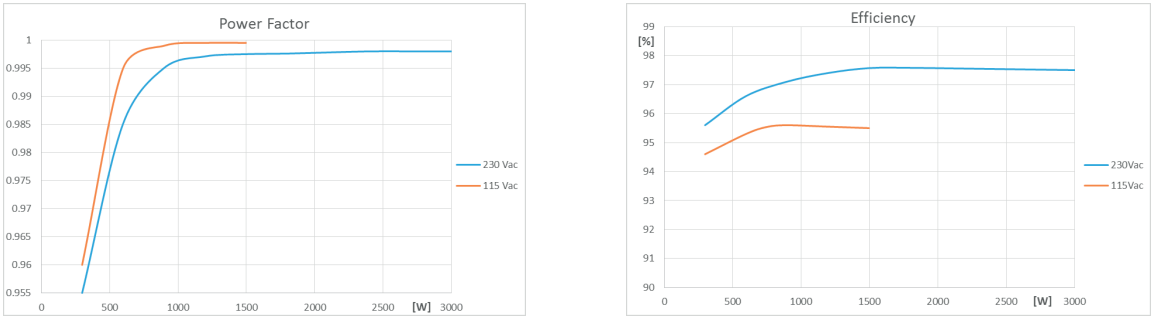

Figure 14 *Power factor vs output PFC power (left) and converter efficiency (right)*

cycle by cycle regulation and the flexibility of a digital system still performing high effiency.

In the paper, theoretical aspects have been considered, the design of both the analog and the digital control loops is introduced and the procedure for the control implementation has been provided.

A prototype has been realized in order to test the proposed control scheme. THD of 3 % and PF well above 0.99 are achieved for the rated power, the measured efficiency at 230 Vac is just below 98 % and shows a nearly flat behavior. Moreover, input current waveform is not affected from grid voltage distortion and test results show very good performances for both steady-state and dynamic conditions.

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