NODE RINGING REDUCTION OF SYNCHRONOUS BUCK CONVERTER

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Resume
This paper discusses the issue related to the switching regulators operated at high switching frequencies, where it is necessary to eliminate the influence of parasitic components of the converter's main circuit. In more detail it deals with the node-ringing phenomena, which is typical for synchronous buck converters. The existence of the parasitic inductances arising from the printed circuit board conductive paths, induce voltages, which are several times higher than nominal input voltage, thus it increases the risk of damage of the power transistors. Therefore, optimization of the circuit is required to reduce the voltage spikes and therefore improve safety margin related to nominal operation. In this paper, node-ringing phenomena is introduced, while the optimization methodologies for its reduction are described and verified by experimental analysis.

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1 Introduction

Current situation in the field of power electronic systems records massive expansion concerning breaking the usual trends. Here we are talking about development of the power semiconductor devices, while significant results are being achieved in terms of performance improvements, as well. The silicon carbide (SiC) is currently leading technology for high-voltage applications, such as electric vehicles, power supplies, motor control circuits and inverters for renewables. This technology offers several advantages over the standard silicon-based power semiconductor devices (IGBT, MOSFETs), which have been used for a long time as the main solution, due to their cost-effectiveness (Figure 1). Due to increasing demands on power density and efficiency of the power systems, the advent of new technological solutions represents a natural process of modernization of all the conventional, as well as specific performance electronic systems [1-3].

Designers of new, more demanding applications such automotive electrical systems and electric vehicles concluded that the new SiC and GaN technologies of power semiconductor structures, with their properties, are more suitable to achieve the desired results [4-5].

Just as modern technologies provide benefits, the use of modern devices also brings certain risk and pitfalls. As was mentioned, power - supply efficiency becomes increasingly important, meeting the high power densities means increasing the switching speed, so the negative trade-offs, like the electromagnetic interference, may occur (Figure 2). Here it is very sensitive issue, which is directly connected to practical design of any power converter, i.e. the printed circuit board (PCB) design represents the design challenge to prevent any unwanted phenomenon. In connection to requirements defined for modern power supplies, the high switching frequencies are required for their operation. One of the negative consequences when dealing with the PCB design and high frequency operation is generation of so-called node-ringing. Parasitic elements of the PCB or device package are responsible for transistor voltage node ringing, which should be optimized to prevent from damage of the component. The effects of these parasites are unexpectedly large and it often happens that a circuit, even if designed without problems, may

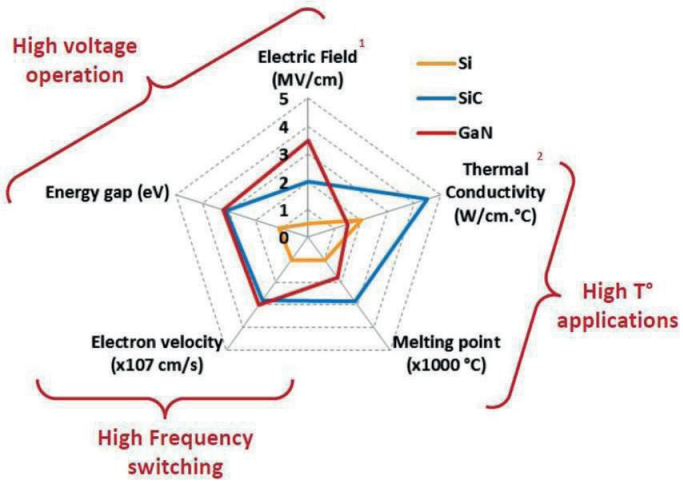

Figure 1 *Comparison of the electrical and operational properties of Si, SiC and GaN technologies of power semiconductor devices*

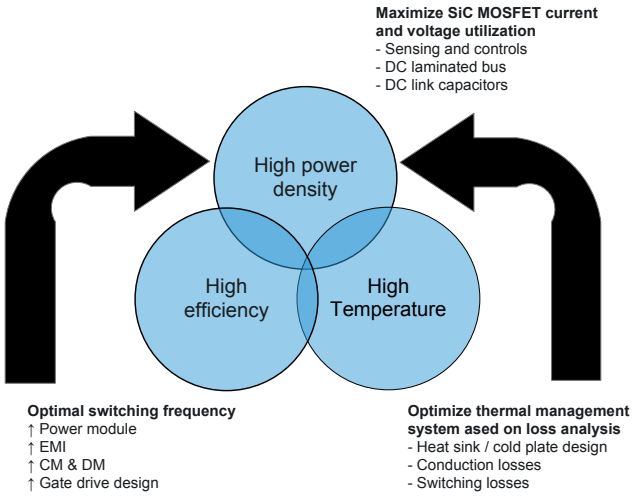

Figure 2 *Diagram representing key demands on the switched mode power supplies*

not operate properly, depending on the layout, due to insufficient attention being paid to these parasitic components [6-7].

In this paper, the focus is given on analysis of the node-ringing origin and its consequence regarding the power loss generation. The study is performed with synchronous buck converter, whose application is redundant power supply system. Initial analysis of the node-ringing is consequently modeled using verified circuit simulation model, while several methods how to the reduce node-ringing phenomenon are being described, as well.

2 Reasons of the node ringing generation

2.1 Main circuit desctiption regarding the node ringing generation

Increasing number of industrial applications, require low output voltage/high current converters. That is related to efficiency maximization, so the buck regulators are of interest when dealing with the power loss minimization. The high output current applications are specific, since the modular converters operated in parallel are utilized to reduce the thermal stress of power components. To be able to provide reliable and safe operation, the minimization of any negative phenomena is a must, while the node-ringing represents a major issue, which must be eliminated for buck regulators operating in a modular system.

Figure 3 shows the principal schematics of synchronous buck converter including the parasitic components of the main circuit. Those are inductances of wirings of PCB and capacitances, which are parasitic components of power transistor itself. The presence and the effect of these parasites is the matter of this research, more precisely the way how to reduce their impact is the main issue. During the converter operation, they are responsible for unwanted oscillations of voltage and current waveforms and the result is overvoltage and overcurrent spikes generation, which negatively affect

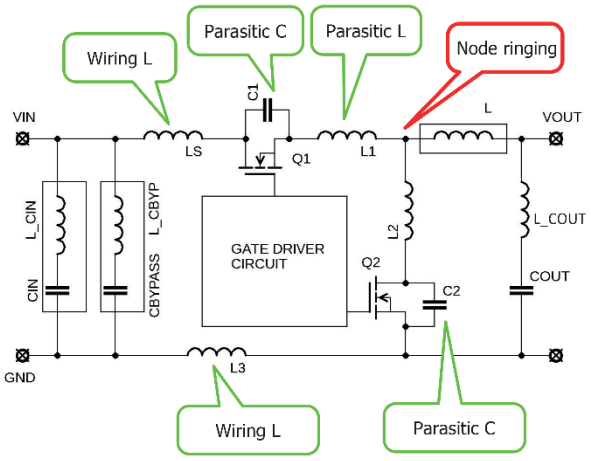

Figure 3 *Principle schematic of synchronous buck converter including the parasitic components*

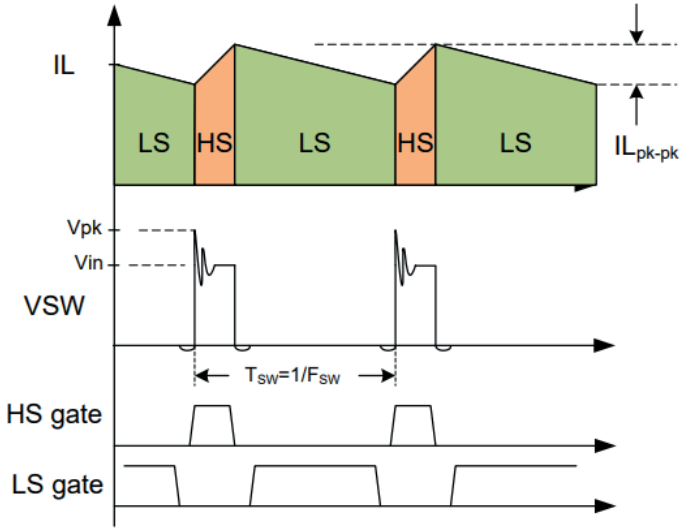

Figure 4 *Time waveforms of synchronous buck converter indicating the node-ringing voltage*

the electromagnetic interference of the power system.

Figure 4 shows time waveforms of converter shown on Figure 3, introducing node-ringing effect, what is seen at the waveform of bottom power switch drain-source voltage.

The principal operation of the synchronous buck converter, operated in continuous conduction mode (CCM), considering nominal conditions, is based on the alternative high-side MOSFET and low-side MOSFET conduction of inductor current during each switching cycle. Cycle initialization is characterized by the green interval when low-side transistor is turned and is carrying the inductor current. After that, the LS MOSFET is turned off and the inductor current is freewheeling through the body diode of the low-side MOSFET. After a short dead time, the HS MOSFET switches on, starting the next conduction interval of inductor current. As the body diode undergoes reverse recovery, the voltage on SW begins to rise and the ringing waveform results from the interaction of parasitic inductances and the switch node capacitance (primarily consisting of the C_{OSS} of the low-side MOSFET) [8]. It must be noticed here that the overvoltage spike caused by node ringing can achieve multiples of the nominal blocking voltage of the transistor, thus possibly leading to its destruction. The amount of this spike directly depends on the value of parasitic inductances of wirings and the reverse recovery of used power semiconductor component [9].

Secondarily, the node-ringing effect affects the operational efficiency of the converter itself, therefore it is worth to deal with the elimination or reduction of the causes that are responsible for the generation of this undesirable phenomenon.

3 Physical prototype of analyzed synchronous buck regulator

Analyzed converter topology is synchronous buck rectifier with interleaved topology. Figure 5 shows the physical prototype of one synchronous buck module,

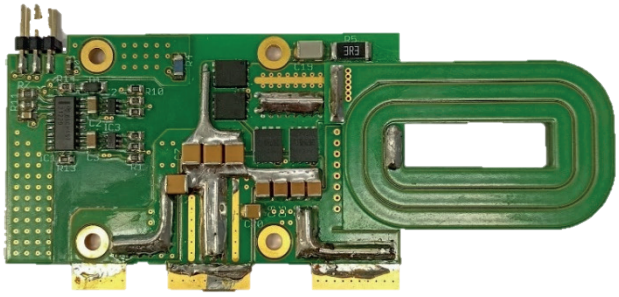

Figure 5 *Module of power converter*

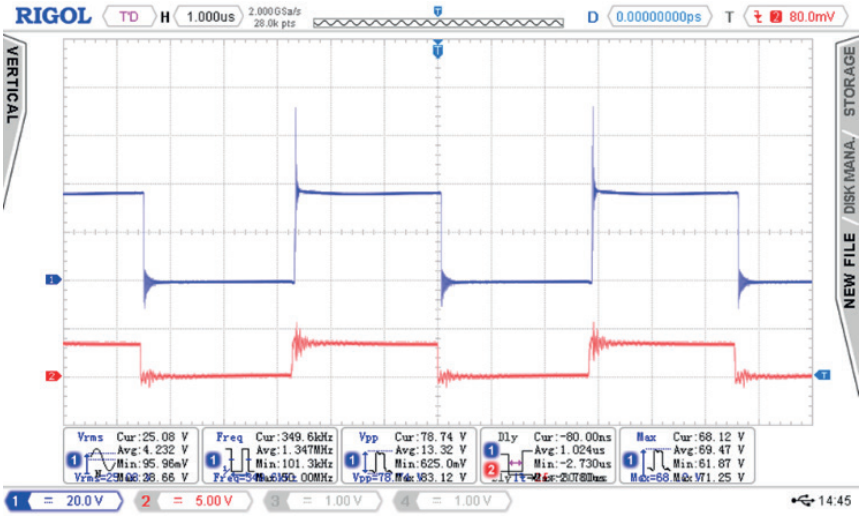

Figure 6 *Drain to source voltage waveform (top) for nominal power of synchronous buck regulator module from Figure 5*

while when it serves for the modular PSU design it contains two. The phase delay between switching of those modules is 180° to reduce the output voltage and current ripple. The modular PSU is designed for supplying the high-power ASIC microchips or high power MCU's where the low voltage and high currents are requested. The modules are constructed on the 6-layer FR4 printed circuit board, where the thickness of internal copper layers is 105 µm and external layers are plated to thickness of 130 µm. The bottom side of PCB is equipped by aluminum heatsink for cooling the power transistors.

Basic parameters for one module:

- Nominal input voltage: 36 V
- Output voltage: 12-22 V
- Maximal output current per module: 35 A
- Maximal output power per module: 600 W
- Maximal eficiency of module: 98.8 %
- Power transistors: 027N10N6 (Infineon)

The complete PSU contains 3 channels (6 power modules) where the maximal output power of one channel is 1200 W and then the maximal output power of whole PSU is 3600 W. As described earlier, the node ringing is one of the problematic issues, which needs to be optimized in buck synchronous regulators. For designed physical sample, measurement of the drain-source voltage of the low-side transistor (Figure 6) indicates, that the optimization should be performed here, as well. The value of the voltage spike, generated on the low-side transistor, is twice the value of the input voltage, i.e. 72 V. In the next part of this paper, two alternatives for optimization are being analyzed, while efficiency of the converter and drain-source voltage peak reduction are the main variables, which are evaluated.

4 Simulation analysis of the node ringing reduction

For the purposes of evaluation, which procedure represents effective solution for the node ringing reduction, it was decided to design the verified simulation model with high level of accuracy [10-12]. For this purpose, the development of the PSpice circuit was performed utilizing highly accurate models of power transistors (ST microelectronics - STL135N8F7AG), which are equipped within physical prototype, as well. The simulation model of the main power circuit is shown in Figure 7. Main circuit contains parasitic components as well, which are responsible for the node ringing generation (stray inductances).

From initial simulation result (Figure 8) it is seen that the voltage spike, generated during the transistor switching, is reaching twice the voltage of the DC supply

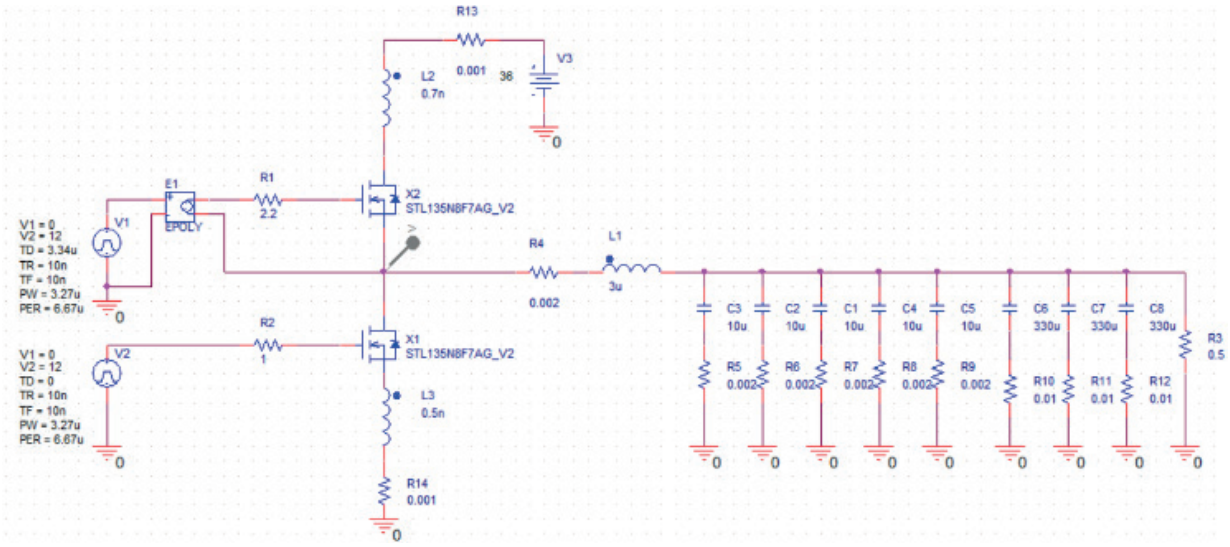

Figure 7 *Simulation model of the considered synchronous buck regulator for the node ringing reduction analysis*

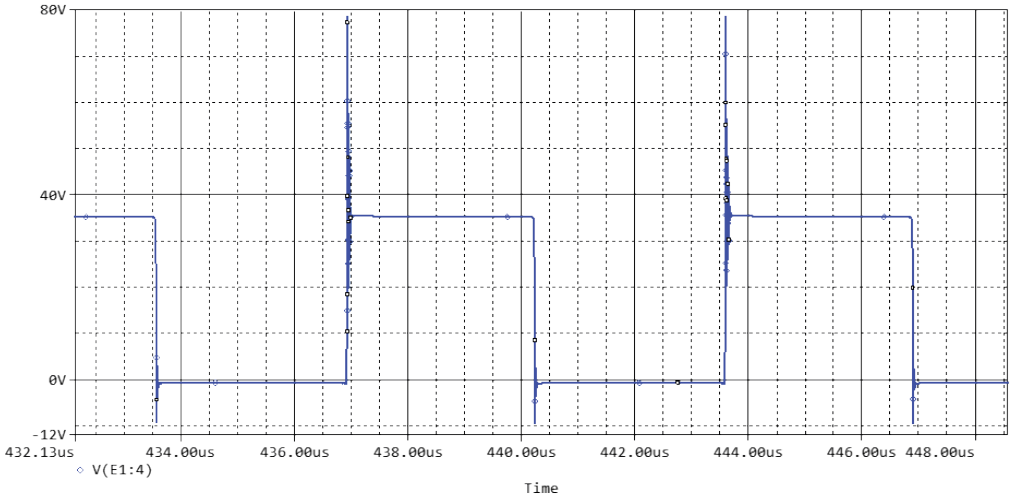

Figure 8 *Simulation result for the drain to source voltage waveform for nominal power of synchronous buck regulator module from Figure 7*

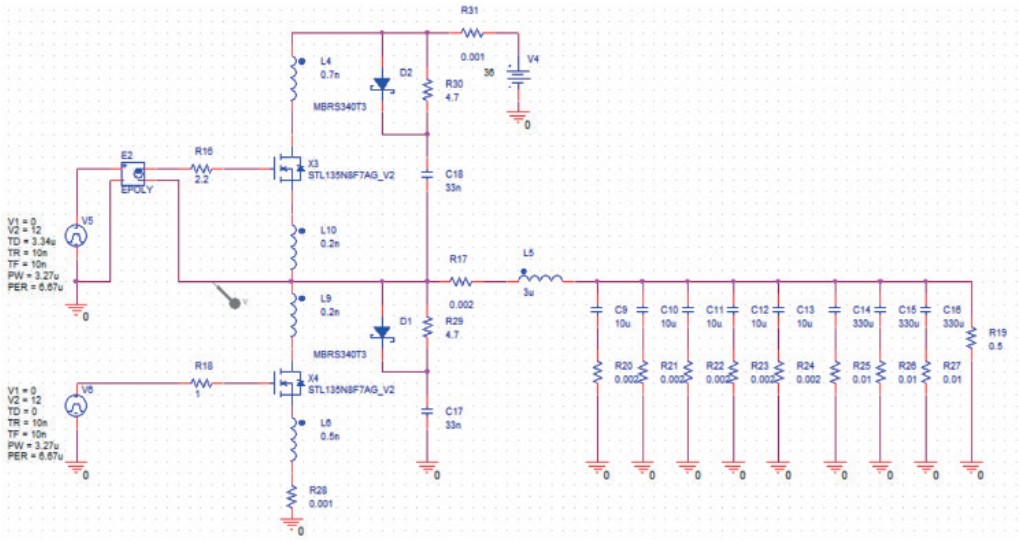

Figure 9 *Simulation model of the considered synchronous buck regulator with snubbers for the node ringing reduction analysis*

voltage. Comparing this result to the measurement (Figure 6), it can be deduced that the result is verified and similar, so the optimization procedure would give the adequate results and information for the optimization needs. We have analyzed two methodologies for the node ringing reduction:

- Slowing the turn-on of the low-side transistor (25 % slow down compared to non-optimized)
- Using the snubber circuits (for studied case: R = 4.7 Ω, C = 33 nF, D = MBRS340T3 Schottky)

According to the first method, reduction of the transistor switching speed may reflect within the increase of the total switching losses of the device, because the transition within the linear region of the volt-amp characteristics is lasting longer. Therefore, the optimal compromise between the reduction of ringing voltage and increase of switching loss must be met. Regarding the second method, it is expected that the power losses of the converter would increase due to fact, that the RCD snubber represents passive snubber circuit dissipating the energy coming from the node-ringing oscillations.

The simulation experiments for the first method have been realized using schematics shown in Figure 8, while for the second method schematics from Figure 9 was used.

As was initially mentioned, two variables are under investigation, i.e. efficiency within the whole power range and drain - source voltage peak caused by the node ringing. Figure 10 shows dependency of the efficiency on output power, while the non-optimized converter is compared to applied methods for the node-ringing reduction. It is seen from the results, that the highest efficiency is achieved for the non-optimized solution. The lowest value of the efficiency within whole power range states for the RCD snubber method, what reflects increased energy dissipation due to RCD snubber functionality, i.e., it dissipates the energy originating from the node ringing overvoltage. If slowing the low-side transistor turn on the process, higher efficiency is obtained, while for 100 % P_{OUT}, the value is 95.24 % what is 1.38 % lower compared to non-optimized solutions and 0.73 % higher compared to the RCD snubber result.

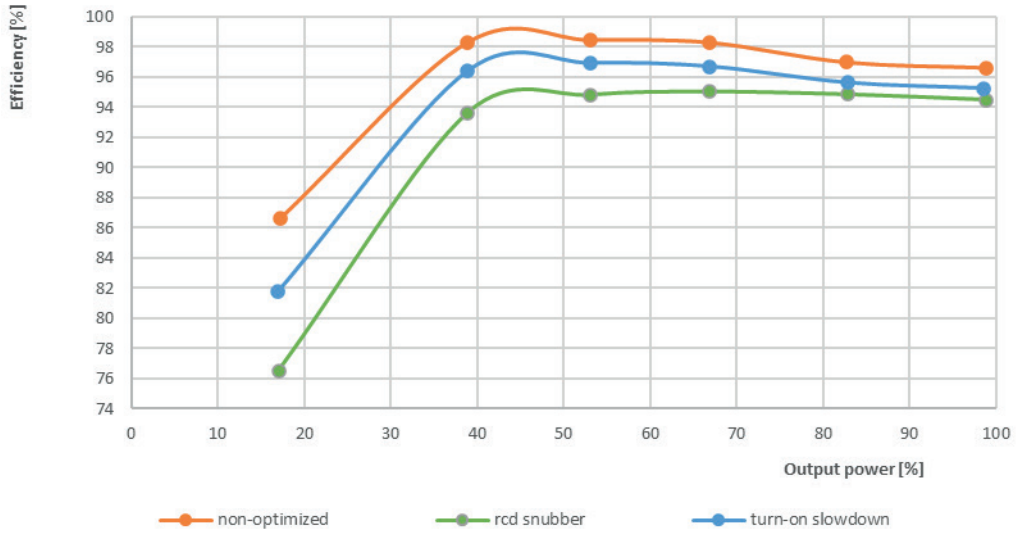

Figure 10 *Efficiency dependency on the output power of the studied converter for the non-optimized sollution and two investigated approaches*

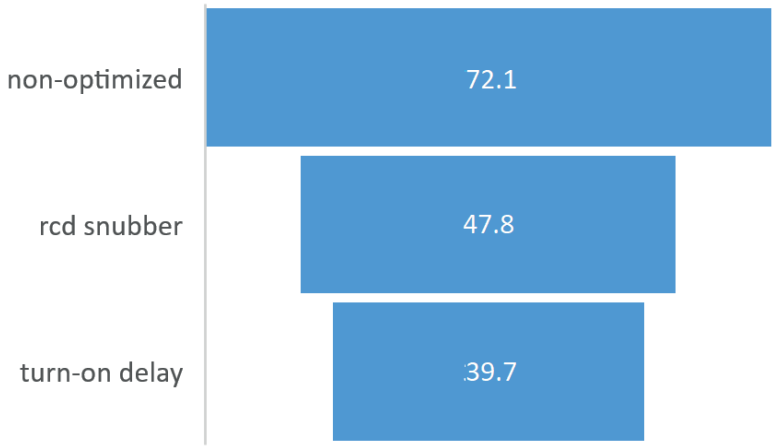

Figure 11 *Voltage spike value for individual study cases*

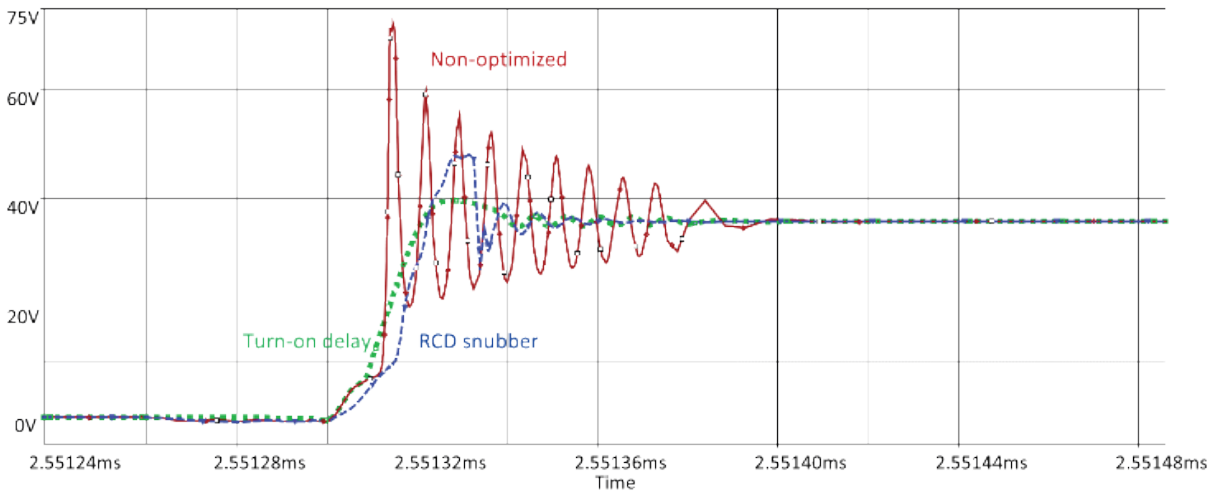

Figure 12 *Time waveform of node-ringing voltage for studied converter and optimization methodologies*

Figure 11 is showing evaluation of the results related to the drain-source peak voltage for the low side transistor of synchronous buck converter. The nominal input voltage is 36 V, while from the results it is seen that the non-optimized solution reached twice the value of input voltage. Considering the RCD snubber, the reduction of the voltage spike by 34 % was achieved, while for the turn-on delay method, reduction reached 45 %. The time waveforms comparison of these results is shown in Figure 12.

5 Conclusion

In this paper, the verification of methodologies for the node-ringing reduction has been the main focus of interests. Initially, discussion, related to the current progress within the power semiconductor technology development, was provided; followed by the description of the synchronous buck converter, the phenomena of node-ringing generation were introduced, as well. It was presented that this issue is dangerous considering the overvoltage damage of the power transistor used within the main circuit. Optimization for reduction is therefore required, while several methodologies are already available. Instead of the printed circuit board layout optimization, there are also other methodologies, which are based on the circuit modification. Here two alternatives have been verified. Once the prototype of the power converter was presented, the node-ringing voltage was measured as well to see the amount of overvoltage generation. The voltage spike reached twice the value of the input voltage of the converter. This result shows, how important it is to prevent from overvoltage damage, when the node-ringing is present. Another issue is electromagnetic emissions (EMI) optimization as well. The evaluation of the optimization methodology influence was provided through the verified circuit simulation model. We investigated the RCD snubber application and methodology, which is characterized by the turn-on slowdown of low-side transistor. The achieved results evaluated the efficiency performance for individual study cases and the amount of voltage spike reduction. From the results is seen that the turn-on slowdown improves voltage spike reduction by 45 % compared to the non-optimized solution. On the other hand, it was negatively reflected in the reduction of efficiency by almost 1.4 % compared to the non-optimized solution. As a conclusion it must be deduced that the node-ringing phenomena is unwanted as it harms the performance of the converter, from the EMI point of view, as from the safe and stable operation.

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Conflicts of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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