EVALUATION OF SILICONE CARBIDE MOSFET DRIVING CIRCUIT PERFORMANCE

Veronika Švárna, Michal Frivaldský*

Department of Mechatronics and Electronics, Faculty of Electrical Engineering and Information Technologies, University of Zilina, Zilina, Slovakia

*E-mail of corresponding author: michal.frivaldsky@uniza.sk

Michal Frivaldsky 0000-0001-6138-3103

Resume

The performances of different driving circuits configurations designed for silicon carbide MOSFET transistors are compared in this research. The simulation of the double-pulse test (DPT) was performed with the use of three driving circuit configurations. The SiC MOSFET NTH4L022N120M3S has great dynamic parameters, which made it suitable for the DPT simulation. It was performed with six different driving voltage ranges, all within the range between -10 V and 20 V. The results were taken across the wide range of driving resistances placed between the driver and the SiC MOSFET, where the switching losses were taken. Drawing from the observed measurements and derived plots, the optimal UGS driving interval for managing the SiC MOSFET transistor is determined to be -10 V/20 V when using a circuit design that incorporates both turn-on and turn-off resistors and diodes.

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1 Introduction

In this paper is discussed how the configuration of the driving circuit affects the switching performance and power losses of high-end SiC power transistors. To analyze the impact of gate drive topology, accurate, validated simulation models and the simulation-based methods were utilized. The results show that a well-designed driving circuit configuration can optimize power loss in the transistor, thereby improving the thermal performance of the power semiconductor converter.

Presently, the silicon-carbide MOSFET transistors are becoming increasingly popular, and, in many applications, they are taking over the role of the switching component instead of classic silicon MOSFET transistors, [1]. Although both devices are metal oxide semiconductor field effect transistors, intrinsic electrical properties of silicon-carbide material introduce the need for the driving circuits with the properties optimized for the new material. Silicon carbide (SiC) power devices offer high switching speeds that enhance efficiency, power density, and overall performance. However, their unique characteristics require careful gate driver design to ensure optimal switching behavior, [2].

With the improved properties and advantages come a few drawbacks that need to be taken into consideration. SiC-MOSFETs are well-suited for power converters due to their superior performance, but their fast switching can lead to surge voltages, spike currents, and EMI problems. Therefore, optimizing the gate drive circuit is essential to fully harness their capabilities while minimizing adverse effects, [3]. One of many interesting features of SiC MOSFETs is the ability of inverse conduction, [4]. However useful the feature is, consequently, it influences the efficiency of an application and power losses, [5]. The detailed examination of the gate drive requirements for SiC-MOSFETs is essential to mitigate the risk of undesirable events leading to unintended switching or excess switching losses, [6].

The complex design of a gate driver depends on whether it operates a high-side or low-side MOSFET, with low-side drivers being simpler due to their ground reference. High-side drivers require additional components to handle varying source potentials, [7]. Furthermore, the distinct characteristics of SiC MOSFETs demand tailored driver circuits to ensure the proper functionality and performance, [8].

In this work is explored how different gate driver

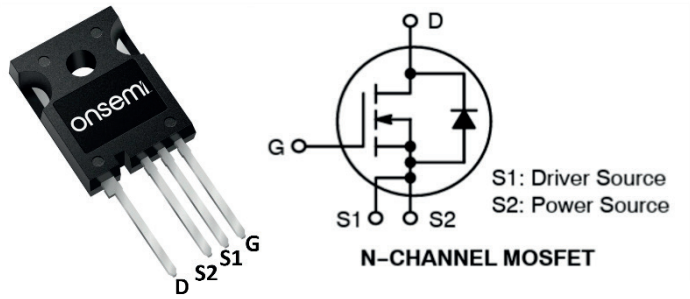

Figure 1 *The silicon-carbide based MOSFET NTH4L022N120M3S from onsemi (left: real-life image, right: schematic symbol with description)*

configurations affect the switching losses of a high-performance 1200 V SiC power transistor. The analysis relies on time-domain simulations using detailed non-linear SPICE models to ensure accuracy. Three distinct driver setups, along with variations in gate-source voltage amplitude, were evaluated to assess their impact on device performance.

2 The selection of the power MOSFET transistor

Due to the great thermal and electrical properties, the silicon-carbide MOSEFT NTH4L022N120M3S from onsemi was selected. This transistor shown in Figure 1, represents the latest generation of the SiC power transistors with the planar manufacture technology aiming the best-in-class operational performance. Instead of that, a wide portfolio of the PSpice libraries is available for simulation purposes, while these models are exhibiting verified and accurate electro-thermal behavior. With the focus given on the simulation research methodology (saving time in relation to laboratory measurements) this was the key factor for the component selection.

This MOSFET has a breakdown voltage of 1200 V, and it is capable to withstand the maximum drain current of 89 A. The typical on-state resistance of the MOSFET is 22 mΩ at 18 V. The recommended operation driving voltage range is -3 V to 18 V and the absolute maximum voltage range allowed on the gate is from -10 V up to 22 V. It is suitable for high switching speeds because of its very low total gate charge of 137 nC, [9]. A key advantage of this MOSFET is its TO-247-4 package. This package provides excellent thermal performance, with $R_{\theta JC}$ = 0.43 ºC/W and $R_{\theta JA}$ = 40 ºC/W. It also features a four-pin layout. The gate and Kelvin source pins are placed close together to reduce the loop inductance, [10].

3 Methodology - simulation approach

The ideal configuration of the double-pulse test is used for the purpose of simulation. In this configuration, shown in Figure 2, the selected MOSFET is used as lower and upper transistor, while the lower one is the device under the test. The upper transistor is connected in diode configuration with the -3 V DC source connected between the gate and source of the MOSFET. This ensures that the transistor stays closed during the process, and after the first pulse, the current will flow only through the body diode of the upper MOSFET.

The V3 source is connected to the gate through resistors and other simple driving circuits. It was set up to deliver a pair of pulses to activate the gate of the lower MOSFET. The timing parameters, labeled T1 through T8, were fine-tuned for optimal performance. These adjustments ensured that the drain current reached a value of 50 A by the conclusion of the initial pulse.

The selected silicon-carbide MOSFETs are connected in a half-bridge configuration connected to the 400 V DC source. In parallel to this, the capacitor of 500 µF with series resistor of 1 mΩ. In parallel to the upper transistor, the inductor of 80 µH with series resistance of 80 mΩ is connected to upper transistor in diode configuration.

The first tested configuration is simple, one resistor driving circuit. This configuration was chosen due to the reduced size compared to the other driving circuits, and number of components. The major disadvantage of this configuration lies in the resistor alone. It controls both turn-on and turn-off process and all power in this section is dissipated via this single resistor. This may lead to reliability issues and reduced lifespan. Moreover, larger resistor values may lead to a partial gate discharge, increasing the chance of unintended turn-on and failing to adequately suppress oscillations, which makes them poorly suited for high-frequency use. Still, this configuration is preferred in the case of more affordable and simpler solutions if the performance can be neglected.

The second tested configuration, shown in Figure 3, is optimal for the high-frequency MOSFET control, as it allows separate turn-on and turn-off times, improving efficiency, reducing EMI and switching losses, and enhancing stability. Diodes ensure correct current direction but introduce voltage drop losses. Though the more complex and costly, with two resistors and two diodes, proper component selection is crucial.

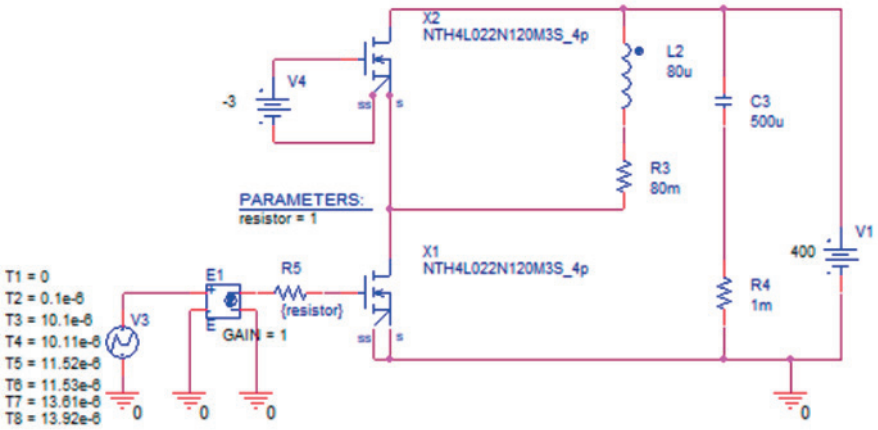

Figure 2 *The double-pulse test schematics using the single resistor gate drive and SiC MOSFET NTH4L022N120M3S*

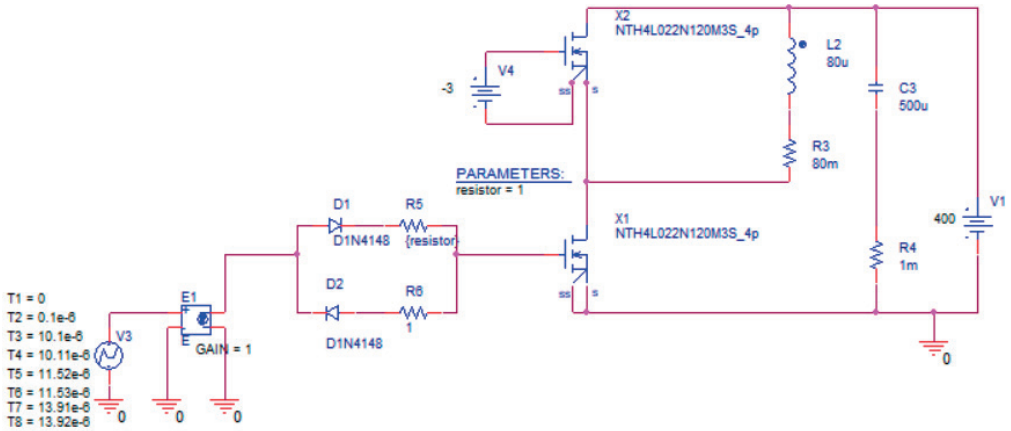

Figure 3 *The double-pulse test schematics using the turn-on and turn-off resistors gate drive and SiC MOSFET NTH4L022N120M3S*

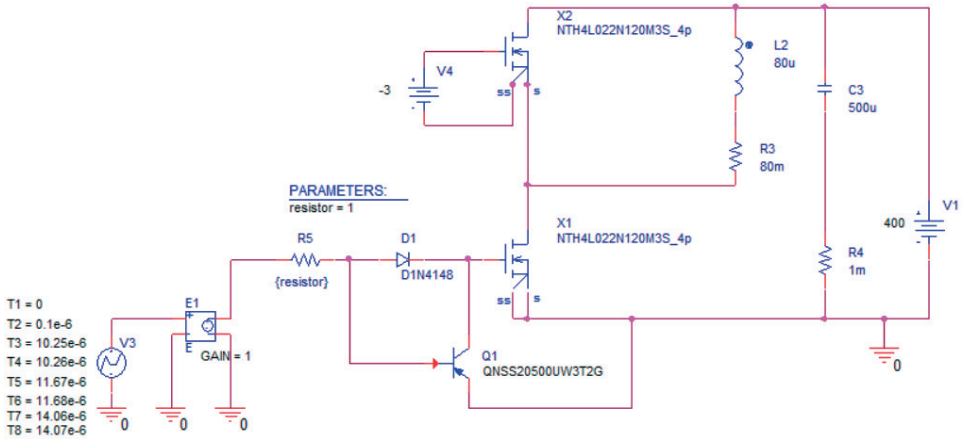

Figure 4 *The double-pulse test schematics using the turn-on and turn-off resistors gate drive and SiC MOSFET NTH4L022N120M3S*

Mismatched values can cause slow switching or high EMI. In this case, the turn-off resistor was fixed based on prior tests, while the turn-on resistor was adjusted within a chosen range.

The third tested configuration, shown in Figure 4, was adjusted to use onsemi PNP transistor NSS20500UW3T2G as a speed-up element. It is rated 20 V, 5 A which makes it sufficient for this application. Though it appears straightforward, this setup demands precise execution. Choosing unsuitable transistors or resistors can greatly impair functionality. Nevertheless, it remains the most common speed-up circuit used in real-world applications. It has several advantages such as easy implementation and control and simple

topology. The major advantage, however, is the element's direct connection to the source of the SiC MOSFET and its capability to discharge the gate of the MOSFET faster. Despite this, the speed-up element elevates the complexity of the driving circuit and overall energy losses which lead to lower efficiency. The design of this kind of driving circuit needs to be done properly. Improper design may lead to oscillations at the gate of MOSFET or high current spikes at high frequencies.

4 Results

The results were obtained from the simulation in OrCAD PSpice. which serves as a reliable platform for accurately modelling and analyzing electrical circuits under various conditions. The simulation focused on determining the total energy loss, which was extracted directly from the program's output data related to voltage, current, and power dissipation across transistor during the switching cycle, an example of which is shown in Figure 5. To ensure the theoretical consistency, the total energy loss was calculated using established equations for energy loss in Equation (1) and Equation (2) listed below. This dual approach - using both simulation data and analytical expressions - helps validate the accuracy and reliability of the findings.

$$E_{ON} = \int_{t_{ON_1}}^{t_{ON_2}} V_{DS} I_D dt\,, \tag{1}$$

$$E_{OFF} = \int_{t_{OFF_1}}^{t_{OFF_2}} V_{DS} I_D dt\,. \tag{2}$$

where: E_{ON} - turn-on energy loss, E_{OFF} - turn-off energy loss, t_{ON1} - initial time for turn-on process, t_{ON2} - ending time for turn-on process, t_{OFF1} - initial time for turn-off process, t_{OFF2} - ending time for turn-off process, V_{DS} - drain - source voltage of device, I_{DS} - drain current of device

To test the correct function of this circuit and verify the level of the I_D current at the end of the first pulse, a timing analysis of the circuit was performed in the range of 10 μs and with a maximum simulation step of 1e-6. The details of the DPT waveform are shown in Figure 6.

The resulting graphs were split into two segments: one showing energy patterns for U_{GS} values up to 10 V, and the other extending to 20 V, to maintain readability and distinction. In the legend of each presented graph, the R represents the resistor which resistance was changed throughout the parametric simulation. In the case of turn-on and turn-off resistors, only turn-on resistor, was changing during the simulation. The turn-off resistor had a fixed value of 1 Ω. Figure 7 shows the graph of the turn-on energy losses in different driver circuit configurations across the range of resistor

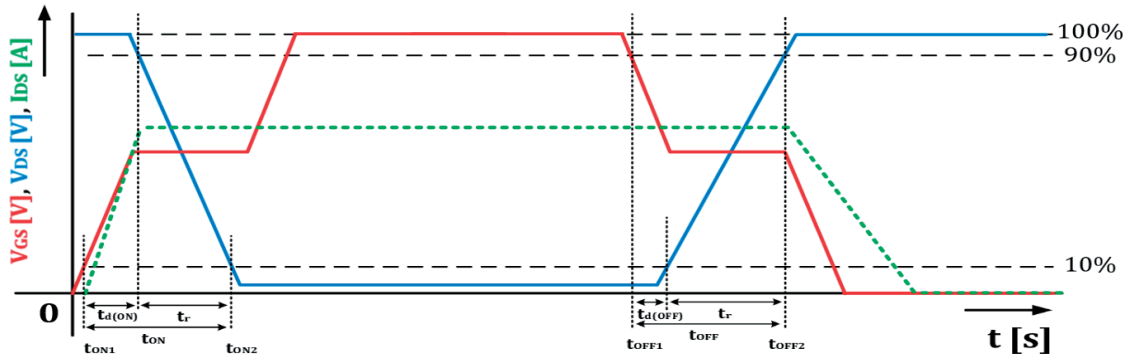

Figure 5 *One switching cycle of SiC MOSFET transistor*

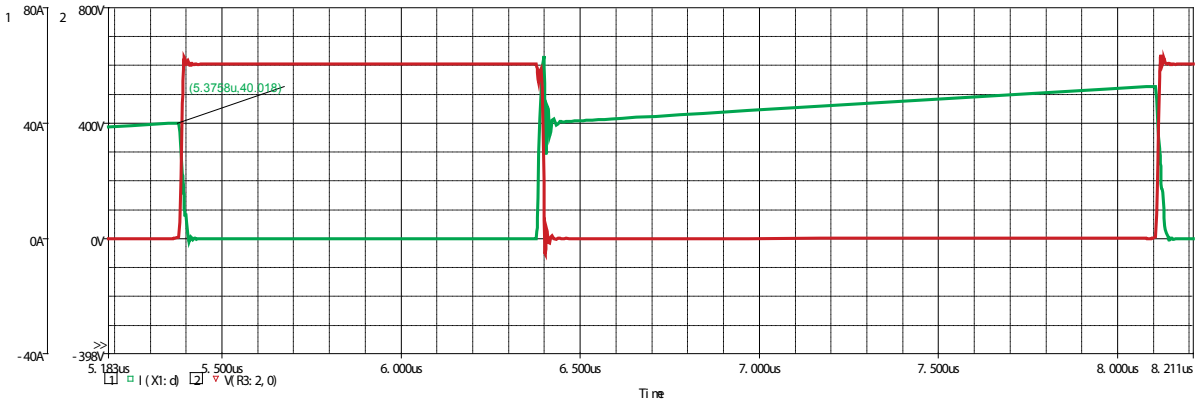

Figure 6 *Example of the simulation DPT result for evaluation of the energy losses*

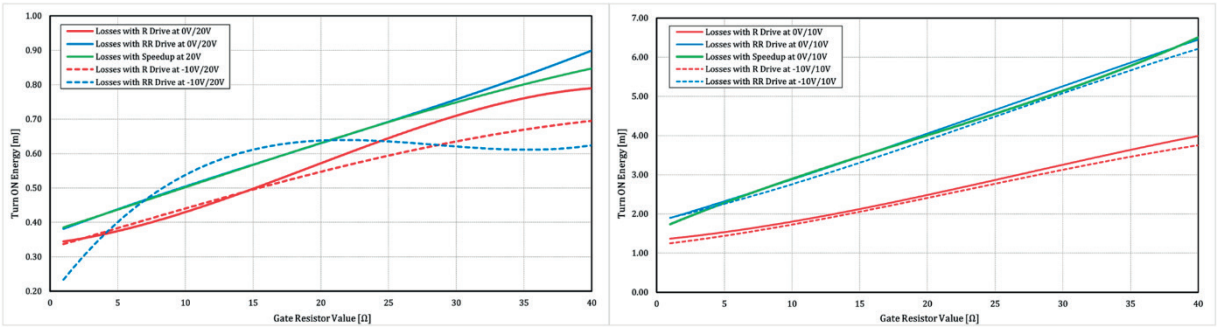

Figure 7 *The turn-on energy losses obtained from the double-pulse test simulation*

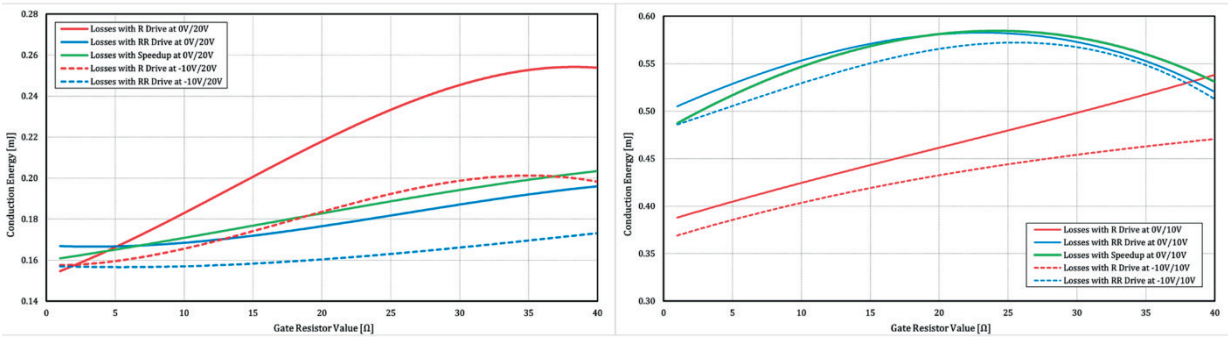

Figure 8 *The conduction energy losses obtained from the double-pulse test simulation*

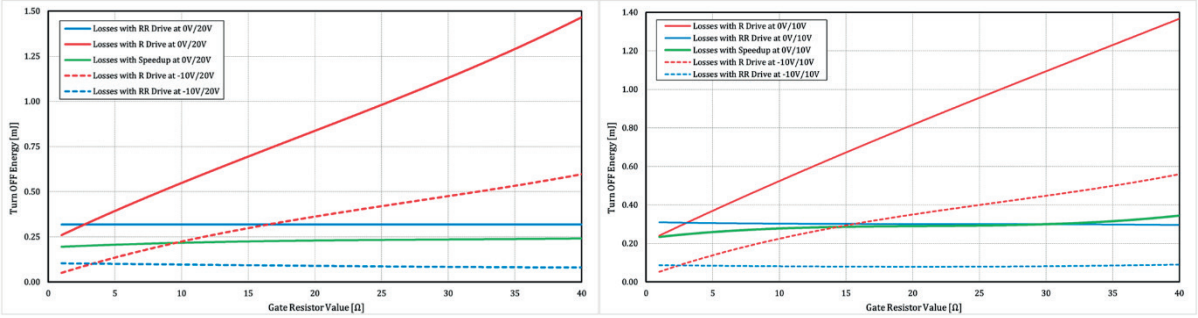

Figure 9 *The turn-off energy losses obtained from the double-pulse test simulation*

values. An analysis of both depicted graphs indicates that the most suitable configuration for the relatively low switching losses is the configuration with single resistor with the driving voltage range of -10 V/20 V in the whole range of selected resistor values. From the lower driving voltage ranges up to 10 V, the most suitable configurations seem to be the ones with turn-on and turn-off resistors within the whole range of selected resistor values. However, the switching loss values with the voltage ranges up to only 10 V were three times higher on average. This same is valid for the conductive, turn-off and consequently, total energy losses.

The graph of the conduction losses, shown in Figure 8, indicates that the most suitable configuration is the one with turn-on and turn-off resistors in the range of driving voltage from -10 V to 20 V. The lowest losses were achieved specifically at 1 Ω but the results show that the losses stayed very low within the whole range of selected resistor values.

The turn-off losses obtained with the driving voltage ranges up to only 10 V were three times higher than those obtained by the driving voltages up to 20 V despite the similarities observed in the graph in Figure 9. Moreover, the results show that similarly to the turn-on, the best option within the tested driver configurations is the one with turn-on and turn-off resistors with the driving voltage -10 V/20 V. The lowest energy loss achieved was recorded at 35 Ω.

The total energy losses (Figure 10) were evaluated and considered separately according to the driving voltage range, up to 10 V and up to 20 V ranges, due to the significant difference in the overall energy loss results. Observing the results in the driving voltage ranges -10 V/10 V, -5 V/10 V, and 0 V/10 V, it is possible to come to a conclusion that the worst configuration in this voltage range category is the one with speed up element, specifically with using 40 Ω resistor at 0 V/10 V driving voltage (7.363 mJ). Opposite to this, the best

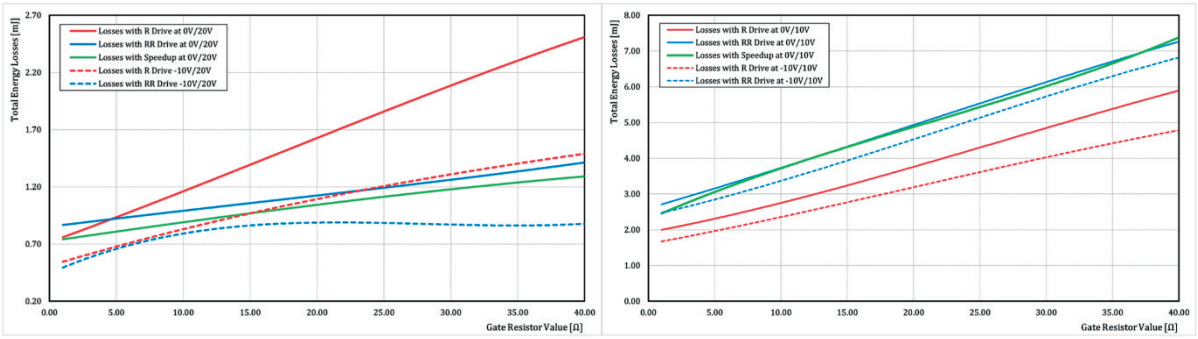

Figure 10 *The total energy losses obtained from the double-pulse test simulation*

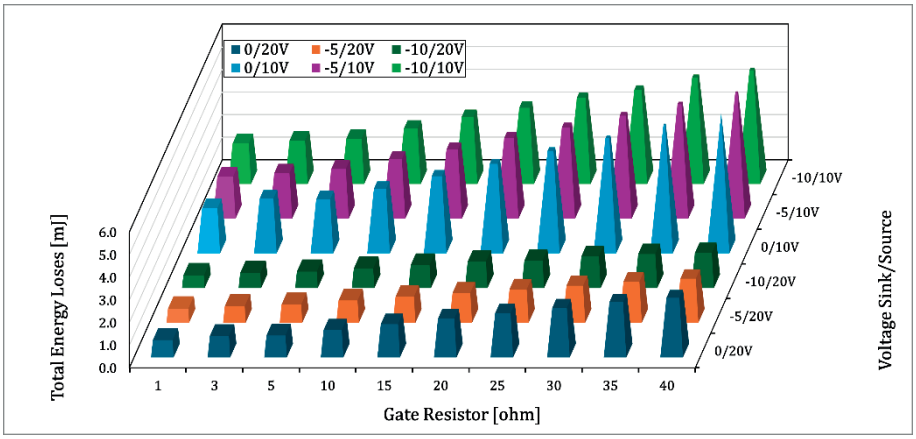

Figure 11 *Total losses at different control voltage ranges in single resistor configurations*

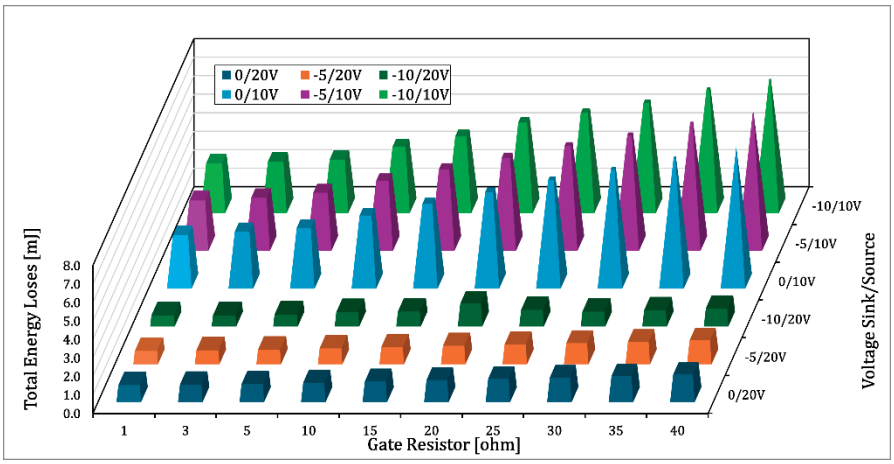

Figure 12 *Total losses at different control voltage ranges in configurations with turn-on and turn-off resistors*

option for tested configurations is the one with a single resistor at -10 V/10 V range (1.705 mJ). As mentioned earlier, the losses in this category are approximately three times higher than the losses in the voltage ranges 10 V/20 V, -5 V/20 V, and 0 V/20 V and therefore the results from this category were more interesting for the overall findings.

The highest losses were observed at the driving voltage 0 V/20 V whilst using at 30 Ω, 35 Ω, and 40 Ω resistors in single-resistor configuration. The best results, in terms of low energy losses were observed in the configuration with turn-on and turn-off resistors at the driving voltage range of -10 V/20 V across the whole range of selected resistors.

The presented results, graphs in Figure 11, Figure 12 and Figure 13, show that the most suitable configuration for controlling the selected MOSFET transistor NTH4L022N120M3S is the one with two resistors using a control voltage from -10 V to 20 V. On the contrary, the worst results were achieved by the

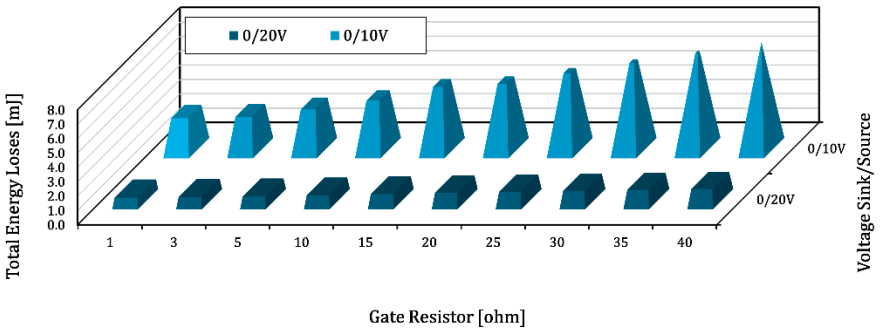

Figure 13 *Total losses at two control voltage ranges in configurations with an accelerating element*

configuration with an accelerating transistor in both control voltage ranges that were simulated, which can be seen in Figure 12.

In general, it is not recommended to use positive voltages lower than 13 V to drive the silicon carbide MOSFETs. This fact results from the physical properties of the structure. This was observed in the high losses at the control voltage ranges of -10 V/10 V, -5 V/10 V and 0 V/10 V in the tables and graphs. With such control, there is a risk of thermal leakage due to high losses and there is also a high risk of false switching due to slower turn-off and a wavy voltage waveform at turn-off.

5 Conclusion

The analysis confirmed the critical importance of proper gate drive voltage selection for SiC MOSFETs, specifically the NTH4L022N120M3S, in power electronics applications. Expanding on this in relation to the current state of technology, SiC MOSFETs are increasingly favored over traditional silicon-based devices due to their superior efficiency, high switching speeds, and thermal robustness. However, their unique physical properties also demand careful optimization of the gate drive circuits. In recent advancements, industry trends continue to reinforce the recommendation of avoiding positive gate drive voltages below 13 V. This aligns with ongoing efforts to improve power efficiency while mitigating risks such as thermal runaway and unintended turn-on. The latter issue, often exacerbated by slow turn-off dynamics and voltage oscillations, has led to further research into innovative gate driver designs. Modern solutions include active gate control techniques that dynamically adjust gate drive parameters to minimize energy losses and improve switching reliability. Additionally, the emphasis on turn-on and turn-off resistors in gate drive configurations remains relevant as engineers strive to refine these circuits for applications in electric vehicles, renewable energy converters, and industrial power supplies. Optimized driving methodologies are being explored to balance the switching speed, EMI suppression, and thermal management, ensuring that SiC MOSFETs can deliver their maximum potential without reliability concerns.

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Conflicts of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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